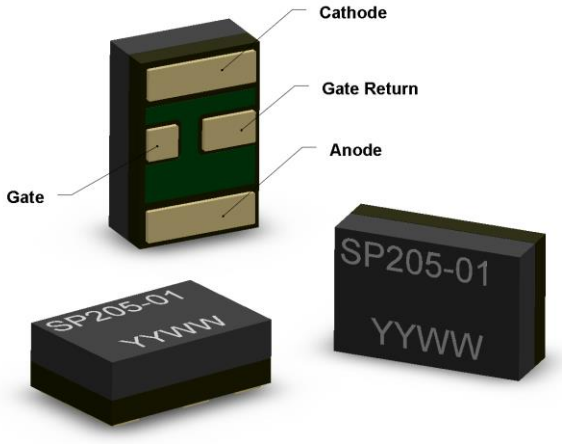
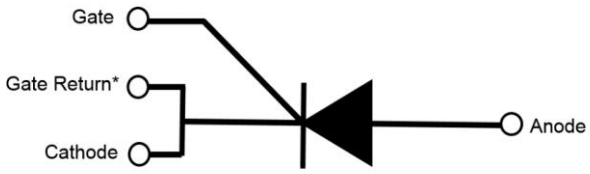
The **SP205-01** is an ultra-fast high-voltage thyristor packaged in an **F-Pak SMT package**. This product is specifically intended for use in initiator applications.

Like the VCS F-Pak product it replaces, the internal semiconductor employs high cell density and an advanced termination design to achieve high peak current capability, low turn-on & conduction loss, very low off-state leakage, negligible turn-on delay jitter, and most importantly, extremely high turn-on di/dt capability. It is also ideally suited for use in a wide variety of other capacitor discharge applications requiring precise timing and rapid charge transfer capability.

The **F-Pak** is a custom surface mount package in which the semiconductor is "flip-chip" soldered onto a high temperature PCB substrate, underfilled then epoxy encapsulated. The package offers a small footprint and low inductance interface that allows for installation using conventional SMT handling equipment.





KEY PRODUCT FEATURES *(Design Intent)*

- 1500V Repetitive Off-State Voltage
- V_{GK} = 0V = OFF
- 120 kA/µs di/dt capability
- Low Turn-on and Conduction Losses
- < 60nSec Turn-on Delay Time
- 3kA Repetitive Anode Current

The **Gate Return pad provides an additional independent connection to the cathode of the semiconductor die. Using the Gate Return pad as a dedicated gate driver return path reduces V=L*di/dt induced stress on the gate drive components.*

Unlike VCS Solidtron devices, the Gate Return pad of CCS devices may, alternatively, be used as an additional Cathode pad; however, using it in this fashion must be qualified by the customer in their specific circuit/application.

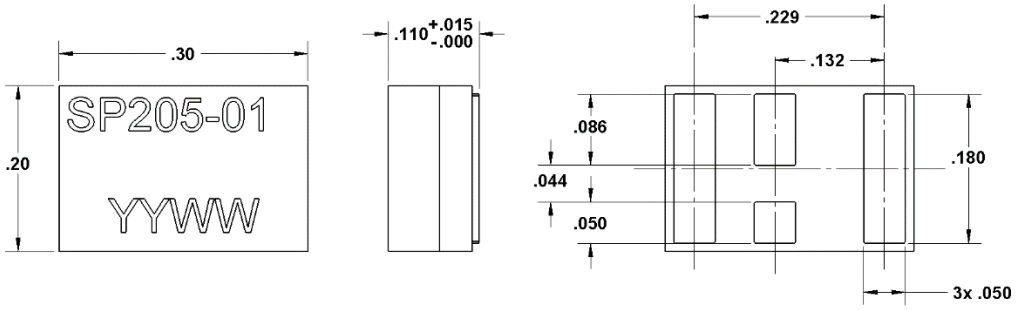
MAXIMUM RATINGS *(Design Intent)*

	SYMBOL	VALUE	UNITS
Repetitive Peak Off-State Voltage	V_{DRM}	1500	V
Repetitive Peak Reverse Voltage	V_{RRM}	-10	V
Off-State Rate of Change of Voltage Immunity (V_D=1500V)	dv/dt	5000	V/µSec
Peak Non-repetitive Surge Current (Sinusoid Pulse Duration=250nSec)	I_{TSM}	4500	A
Repetitive Anode Current (Sinusoid Pulse Duration=250nSec)	I_{TRM}	3000	A
Rate of Change of Current	dI/dt	120	kA/µSec
Continuous Gate-Cathode Reverse Voltage	V_{GKS}	-9	V
Forward Peak Gate Current	I_{GM}	TBD (min. 10A)	A
Required Off-State Gate-Cathode Voltage	V_{GDM}	0	V
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range *(See Moisture Sensitivity & Solderability Cautions)*		-55 to +150	°C

ELECTRICAL CHARACTERISTICS *(Design Intent)*

T_C=25°C unless otherwise specified				Measurements			
Parameters	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Units**
Anode to Cathode Breakdown Voltage	V_{DRM}	V_{GK}= 0V, I_D=100µA		1500			V
Anode-Cathode Forward Off-State Current	I_{DRM}	V_{GK}= 0V, V_D=1500V	T_C=25°C			100	nA
			T_C=85°C			1	µA
			T_C=125°C			10	µA
Reverse Bias Gate-Cathode Breakdown Voltage	V_{GRRM}	I_{GM}=100µA		9			V
Reverse Bias Gate-Cathode Leakage Current	I_{GM}	V_{GK}= -9V			5	20	µA
Gate Trigger Voltage	V_{GT}	V_{AK}= 12V, I_D=1mA		0.4	0.5	0.65	V
Gate Trigger Current (w/ V_{GT} satisfied)	I_{GT}	V_{AK}= 12V, I_D=1mA				1	mA
Input Capacitance	C_{ISS}	Bias=6V, Freq.=120Hz			4		nF
Turn-on Delay Time	$t_{d(ON)}$	0.15uF Capacitor Discharge T_J=25°C, V_{GK}= 0V to V_{GT} V_{DD}=1000V, L_S=10nH, R_{SENSE}=0.010Ω			30	60	nSec
Rate of Change of Current	dI/dt				85		kA/µSec
Peak Anode Current	I_{DM}				3000		A

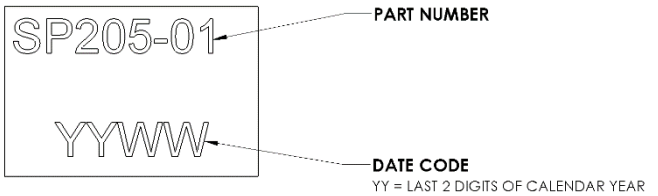
PACKAGE DIMENSIONS



DATE CODE
YY = LAST 2 DIGITS OF CALENDAR YEAR
WW = WORK WEEK OF THE CALENDAR YEAR

DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED:
TWO PLACE DECIMAL +/-0.010 THREE PLACE DECIMAL +/-0.004

MARKING



HANDLING AND STORAGE

ESD Sensitivity

THIS DEVICE IS ESD SENSITIVE. OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC DISCHARGE SENSITIVE DEVICES IN ALL ASSEMBLY AND TEST AREAS (REF. JESD625).

IMPROPER HANDLING OF THIS DEVICE MAY PERMANENTLY DAMAGE THE DEVICE AND RENDER IT UNUSABLE.

Moisture Sensitivity

F-Pak SMD Packages have been qualified IAW IPC/JEDEC J-STD-020D.1 MSL Level 3 SnPb Eutectic Process Temperature (220°C).

Additional higher temperature MSL testing is planned. Results will be published when available.

In accordance with **IPC/JEDEC J-STD-033C**, **F-Pak** products are dry-baked then packed in a Moisture Barrier Bag (MBB) containing desiccant and a Humidity Indicator Card (HIC). When the Moisture Barrier Bag is opened or compromised refer to **IPC/JEDEC J-STD-033C** for proper HIC interpretation, floor life and storage procedures.

Although **IPC/JEDEC J-STD-033C** prescribes specific dry-baking temperatures and times, **CAUTION** is advised as additional baking of **F-Pak** SMD packages may cause increased oxidation and/or intermetallic growth of the terminations, which if excessive, will result in solderability problems during board assembly. The temperature and time for baking this SMD package should, therefore, be limited with solderability considerations in mind.

Solderability

It has been determined that the component pads of legacy **VCS F-Pak** products are ***CONSISTENTLY MILDLY OXIDIZED*** as a result of the manufacturing and required MSL dry-baking processes (Ref. J-STD-033, MSL Level 3, Table 4-2). Customers should be aware that solderability testing of finished dry-baked product indicates that the amount of oxidation present is such that it ***MAY REQUIRE THE USE OF MODERATE OR HIGHLY ACTIVE FLUX*** to achieve satisfactory solder wetting.

PLANNED PRODUCT IMPROVEMENT, unlike the previous VCS device it replaces**,** the new semiconductor die has been designed specifically for F-Pak installation. With this improvement, it is expected that manufacturing heating cycles will be drastically reduced; thus, reducing or eliminating the oxidation noted above.

Samples of the SP205-01 will be tested to solderability IAW IPC/JEDEC J-STD-002C. Results will be published when available.