**SMCT TA 32N14 A10**

Thin-Pak™ Voltage Controlled SolidTRON®

Data Sheet Rev 3 CAO-20140515

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**Description:**
N-Type MOS-controlled thyristor.
Metal surfaces tinned with 63Sn/37Pb solder.
Package is perforated, metalized ceramic substrate attached to silicon die.

**Applications:**
EFD / EFI / ESA / LEFFI / SAF
Capacitor Discharge
Pulse Power

**Features:**
1400V peak off-state voltage
4kA surge on-state maximum current
120kA/us di/dt performance
<100ns turn on delay / no turn-on delay jitter
High peak current capability
Low on-state conduction losses
Low inductance packaging
Solid state reliability
Epoxy underfill to protect high voltage terminals

**Package**

**Use of Gate Return Bond Area**

The MCT was designed for high di/dt applications.
An independent cathode connection or "Gate Return Bond Area" is provided to minimize the effects of rapidly changing Anode-Cathode current on the Gate control voltage, ($V=L*di/dt$).

It is critical the end user utilize the Gate Return Bond Area as the point at which the gate driver reference (return) is attached to the VCS device.
Package Dimensions

![Image of package dimensions]

**Process and Storage**

1. All metal surfaces are tinned using 63pb/37sn solder.
2. Installation reflow temperature not to exceed 260° C.
3. Appropriate to all MOS gated devices, proper ESD handling and storage must be observed.

**Test Profile**

1. Gate Integrity at 25° C and 25 Volts applied is measured as Pass or Fail
2. Di/Dt discharge at 25° C and 1250 Volts is measured for 100 pulses against <100ns and >4Ka specifications
3. Voltage Blocking Stability at 80° C and 1500 V is measured against < 200nA specification
4. Turn on Threshold at 25° C and 12 V is measured to ensure latching <1.5V specification
5. Forward Voltage Drop at 25° C and 10 A is measured against <1.1V specification
6. Gate Integrity at 25° C and 25 V applied is measured as Pass or Fail