C613
40mm Inverter Thyristor
2000V / 475A / 50us

The C613 is ideal for forced commutation. It is processed by multi-diffusion, utilizing 40mm diameter silicon with a unique involute pilot gate. It is supplied in a disk package ready to mount using commercially available heat dissipators and mechanical clamping hardware.

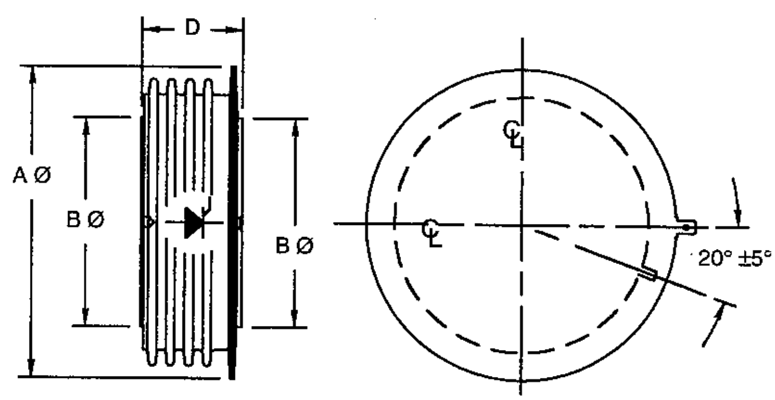
MAXIMUM ALLOWABLE RATINGS

TYPE	V_{DRM}/V_{RRM}[1] REPETITIVE T_J = -40°C to +125°C	V_{DRM}/V_{RRM}[1] REPETITIVE T_J = 0°C to +125°C	TRANSIENT PEAK REVERSE VOLTAGE[1], V_{RSM} T_J = -40°C to +125°C
C613L	2000 Volts	2100 Volts	2100 Volts
C613PT	1900	2000	2000
C613PN	1800	1900	1900
C613PS	1700	1800	1800
C613PM	1600	1700	1700
C613PE	1500	1600	1600

Consult factory for lower rated voltage devices.

Peak One-Cycle Surge On-State Current, I_{TSM} (8.3 msec) .... 6,500 Amperes
Maximum Rate-of-Rise of Anode Current Turn-On Interval[2] .... Switching from 1200 Volts, 500 A/μsec
Repetitive Rate-of-Rise of Anode Current .... Switching from 1200 Volts, 200 A/μsec
I^2t (for fusing) (at 1.5 milliseconds) (See Figure 9) .... 80,000 Ampere^2 Seconds
Peak Gate Power Dissipation, P_{GM} .... 50 Watts
Average Gate Power Dissipation, $P_{G(AV)}$ .... 5 Watts
Peak Reverse Gate Voltage, V_{GRM} .... 20 Volts
Storage and Operating Temperature, T_{stg} and T_J .... Refer Above
Mounting Force Required ....3500 – 4200 Lbs.
15.6 – 18.7 KN

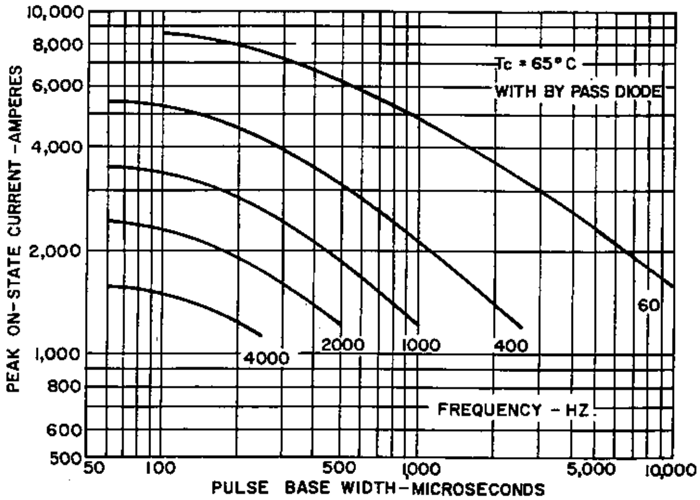
A Ø = 2.30 in (58.0 mm)
B Ø = 1.35 in (34.3 mm)
D = 1.04 in (26.4 mm)



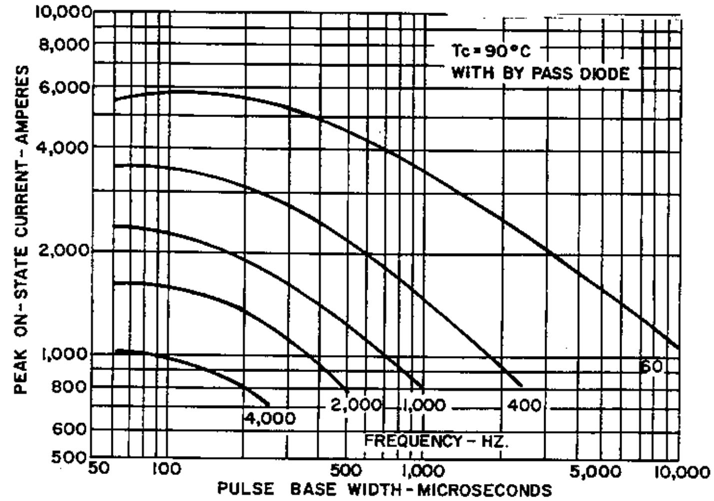
CHARACTERISTICS

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Off-State and Reverse Currents	I_{DRM} and I_{RRM}	–	10	15	mA	T_J = +25°C, V = V_{DRM} = V_{RRM}
Peak Off-State and Reverse Currents	I_{DRM} and I_{RRM}	–	45	60	mA	T_J = +125°C, V = V_{DRM}= V_{RRM}
Effective Thermal Resistance Junction-to-Case	$R_{\theta JC}$	–	–	.04	°C/Watt	Double-Side Cooled (DC)
Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	dv/dt	400	–	–	V/μsec	T_J = +125°C, V_{DRM} = .80 Rated Gate Open[1]
Delay Time	t_d	–	1.6	3.0	μsec	Switching from 900 Volts, 20 Volt, 10 Ohm Gate 0.5 μsec Rise Time, T_J = 25°C
Gate Pulse Width Necessary to Trigger		–	–	10	μsec	See Figure 11.
Gate Trigger Current	I_{GT}	–	120	180	mAdc	T_C = 25°C, V_D = 0 Vdc, R_L = 3 Ohms
		5.0	30	–		T_C = +125°C, V_D = .5 x Rated, R_L = 1000 Ohms
Gate Trigger Voltage	V_{GT}	–	3.5	5.0	Vdc	T_C = 25°C, V_D = 10 Vdc, R_L = 3 Ohms
		.3	–	–		T_C = 125°C, V_D = .5 x Rated, R_L = 1000 Ohms
Peak On-State Voltage	V_{TM}	–	–	2.9	Volts	T_C = +125°C, I_T = 2000 Amps. Peak Duty Cycle ≤ 0.01%
Conventional Circuit Commutated Turn-Off Time (With Reverse Voltage)	t_q	–	40	50	μsec	(1) T_C = +125°C (2) I_T = 500 Amps. (3) V_R ≥ 50 Volts (4) 80% V_{DRM} Reapplied[1] (5) Rate-of-rise of Forward Blocking Voltage = 400 V/μsec. (6) Gate Bias = Open During Turn-Off Interval = 0 Volts, 100 Ohms (7) Duty Cycle ≤ 0.01%
Conventional Circuit Commutated Turn-Off Time (With Feedback Diode)	t_q	–	45	55	μsec	(1) T_C = +125°C (2) I_T = 500 Amps. (3) V_R = 2 Volts Min. (4) 80% V_{DRM} Reapplied[1] (5) Rate-of-rise of Forward Blocking Voltage = 400 V/μsec. (6) Gate Bias = Open During Turn-Off Interval (7) Duty Cycle ≤ 0.01%

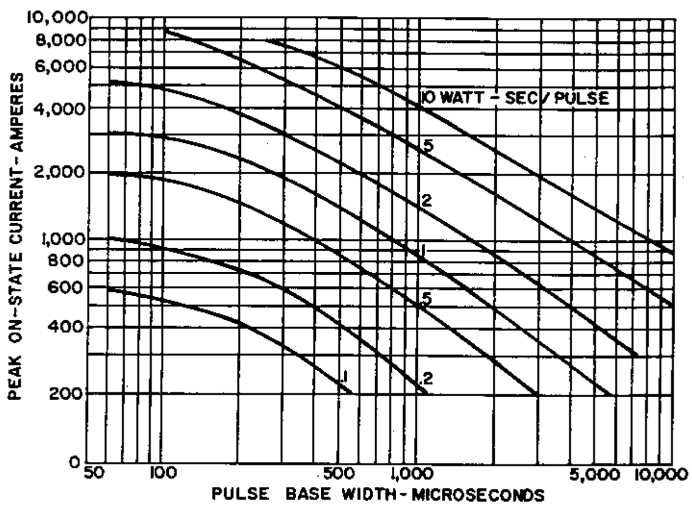
[1] 1 440 V is maximum for C613PT and C613L.



1. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH (T_C = 65°C)



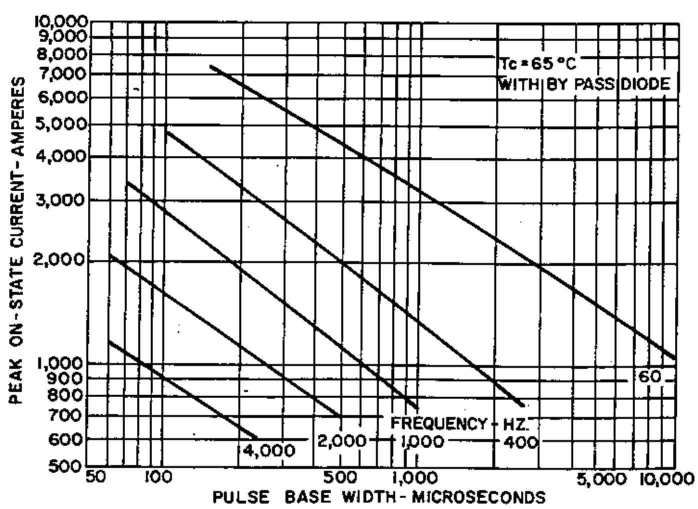
2. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH (T_C = 65°C)



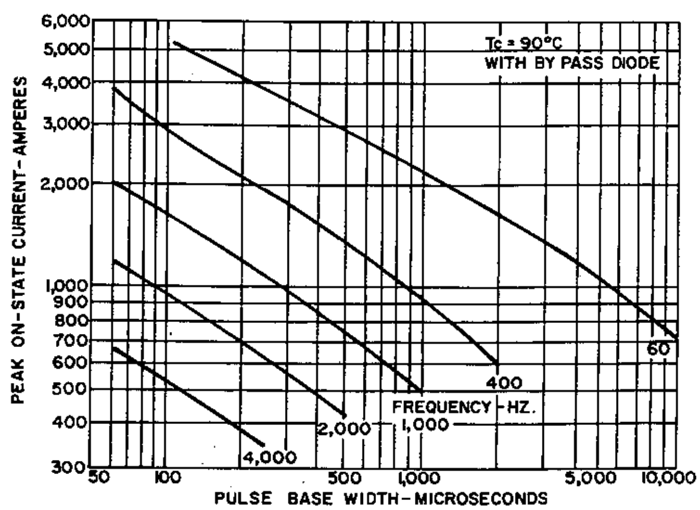
3. ENERGY PER PULSE FOR SINUSOIDAL PULSES

NOTES:

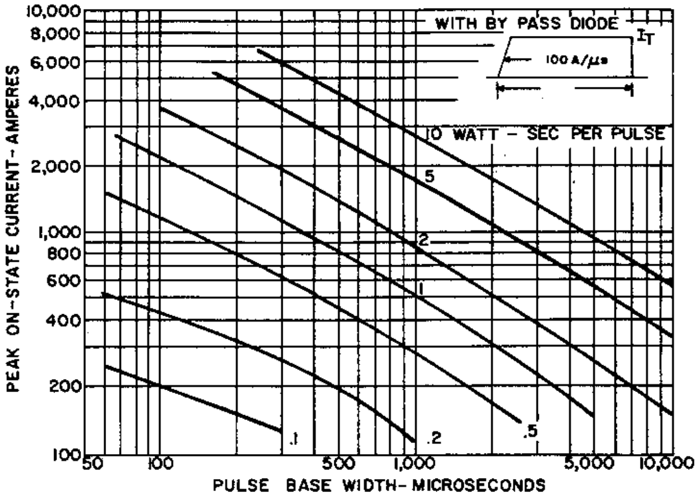
1. Switching voltage range: V_D = 15V – 0.8 V_{DRM}.
2. Peak snubber discharge current ≤ 50A. RC ≤ 10μsec.
3. High gate drive: 20V/10 Ohms, 0.5μsec rise time.
4. Reverse voltage < 50V. If no bypass diode is used, reverse recovery losses must be added.



4. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR RISING DI/DT = 100 A/μSEC. (T_C = 65°C)



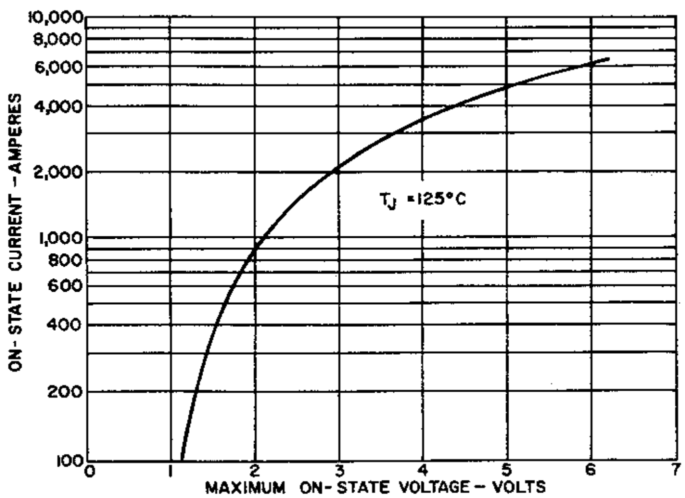
5. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR RISING DI/DT = 100A/μSEC. (T_C = 90°C)



6. ENERGY PER PULSE FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR 100A/µSEC. RISING DI/DT

NOTES:

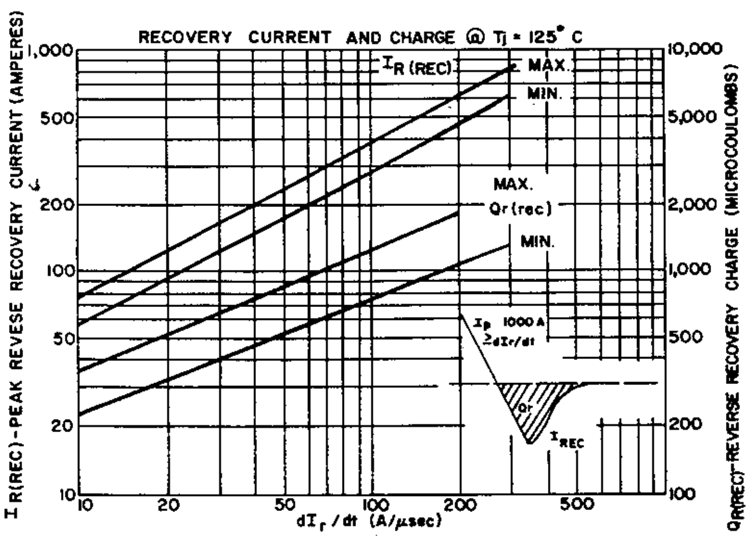
1. Switching voltage range: V_D = 15V – 0.8 V_{DRM}.
2. Peak snubber discharge current ≤ 50A. RC ≤ 10µsec.
3. High gate drive: 20V/10 Ohms, 0.5µsec rise time.
4. Reverse voltage ≤ 50V.



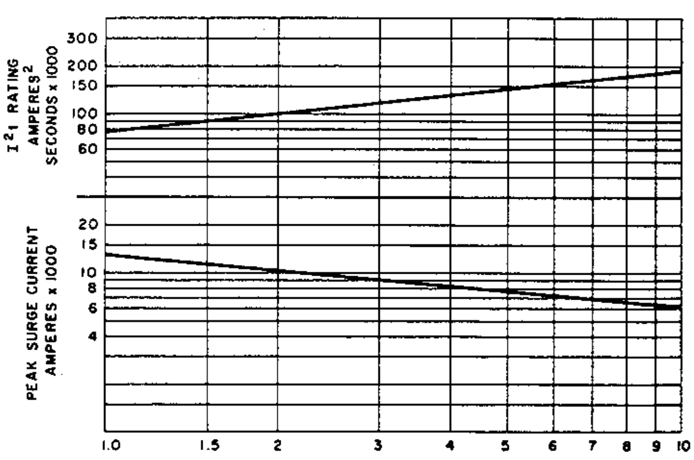
7. FORWARD CONDUCTION CHARACTERISTICS ON-STATE

NOTES:

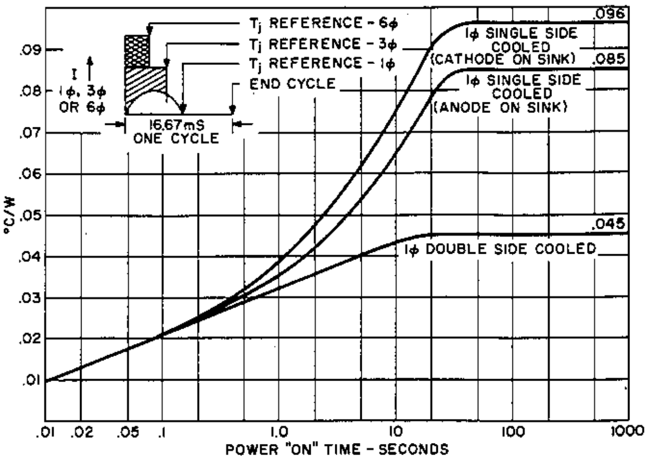
VOLTAGE (Volts)	CURRENT (Amps)
1.145	100
1.300	200
1.423	300
1.533	400
1.634	500
1.731	600
1.824	700
1.914	800
2.002	900
2.089	1000
2.174	1100
2.257	1200
2.340	1300
2.422	1400
2.503	1500
2.900	2000
3.665	3000
4.410	4000
5.142	5000
5.865	6000



8. RECOVERED CHARGE (125°C)



9. SUB-CYCLE SURGE AND I^2t RATING FOLLOWING RATED LOAD CONDITIONS (Sinusoidal Waveform)



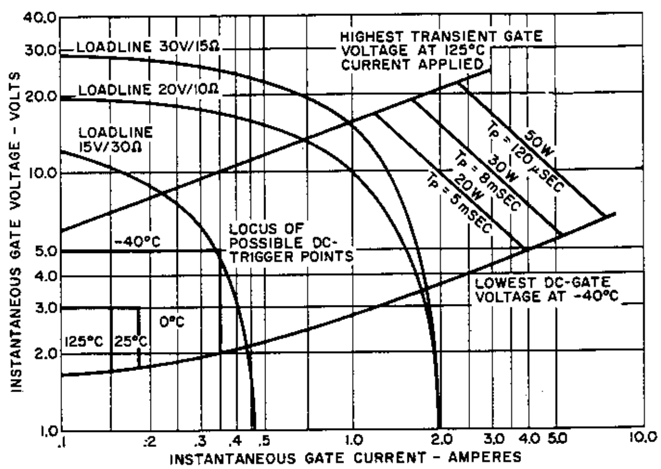
10. TRANSIENT THERMAL IMPEDANCE — JUNCTION-TO-CASE

NOTES:

For 3φ thermal resistance add .0037°C/W along entire curve length.

For 6φ thermal resistance add .001°C/W along entire curve length.

For DC thermal resistance subtract .005°C/W along entire curve length.



11. MAXIMUM ALLOWABLE PEAK GATE POWER VS. GATE PULSE WIDTH

NOTES:

1. Maximum allowable gate dissipation = 3 watts.
2. The locus of possible DC-trigger points lies outside the boundaries shown at various junction temperatures.
3. Loadlines 30V/15 Ω, 20V/10 Ω and similar are recommended as minimum gate drives for most inverter application; rise time ⩽0.5μsec; T_p ⩾10μsec.
4. Loadline 15V/30 Ω is the minimum usable gate drive. Snubber resistances must be > 30 Ω when turning on from ⩾800V bias. Delay-time may be increased. di/dt rating ⩽100A/μsec.