The C713 reverse blocking thyristor is a pressure mounted, high current reverse blocking thyristor designed for power switching. It utilizes an involute interdigitated pilot gate and is manufactured by the proven multi-diffusion process.

Features:

- Off-State and Reverse Blocking Capabilities to 2000 Volts
- Very Low Switching Losses at High Frequencies
- 50 usec Maximum Turn-Off Time at Severe Operating Conditions with Feedback Diode
- Involute, Interdigitated Gate for High di/dt Capability
- Narrow Pulse Capability for PWM Inverter Commutating
- SCR Socket
- 1" Creepage-Path, Glazed Ceramic Package

### MAXIMUM ALLOWABLE RATINGS

<table>
<thead>
<tr>
<th>TYPE</th>
<th>$V_{DRM}/V_{RRM}$</th>
<th>$V_{DRM}/V_{RRM}$</th>
<th>$V_{RSRM}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>REPEITIVE $T_J = -40^\circ C$ to $+125^\circ C$</td>
<td>REPEITIVE $T_J = 0^\circ C$ to $+125^\circ C$</td>
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<tr>
<td>C713L</td>
<td>2000 Volts</td>
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<td>2100 Volts</td>
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<td>C713PT</td>
<td>1900</td>
<td>2000</td>
<td>2000</td>
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<tr>
<td>C713PN</td>
<td>1800</td>
<td>1900</td>
<td>1900</td>
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<tr>
<td>C713PS</td>
<td>1700</td>
<td>1800</td>
<td>1800</td>
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<tr>
<td>C713PM</td>
<td>1600</td>
<td>1700</td>
<td>1700</td>
</tr>
<tr>
<td>C713PE</td>
<td>1500</td>
<td>1600</td>
<td>1600</td>
</tr>
</tbody>
</table>

Consult factory for lower rated voltage devices.

Peak One-Cycle Surge On-State Current, $I_{TSR}$ (8.3 msec) ....................................... 15,000 Amperes

(10 msec) ....................................... 13,500 Amperes

Maximum Rate-of-Rise of Anode Current Turn-On Interval (Switching From 1200 Volts) .......................... 800 A/usec

Repetitive di/dt Rating$^2$ .......................... 200 A/usec

$1^2$ (for fusing) (at 8.3 milliseconds) .................. 933,750 Ampere$^2$ Seconds

Peak Gate Power Dissipation, $P_{GM}$ .......................... 100 Watts

Average Gate Power Dissipation, $P_{G(AV)}$ .......................... 5 Watts

Peak Reverse Gate Voltage, $V_{GRM}$ .................................. 20 Volts

Storage and Operating Temperature, $T_{STC}$ and $T_J$ .................. $40^\circ C$ to $+125^\circ C$

Mounting Force Required .................................. 3000 Lb. + 1000 - 0 Lb.

22.2 KN + 4.4 - 0 KN

NOTES:

$^1$ 10 msec voltage sinewave.

$^2$ di/dt rating established in accordance with EIA-NEMA Standard RS-397, Section 5.2.2. This di/dt is in addition to the discharge of a 0.25 µF, 20 ohm snubber circuit in parallel with the DUT.
<table>
<thead>
<tr>
<th>CHARACTERISTICS</th>
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<td><strong>TEST</strong></td>
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<td>Peak Reverse and On-State Blocking Current</td>
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<td>Effective Thermal Resistance, Junction-to-Case</td>
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<td>Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)</td>
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<td>Delay Time</td>
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<td>Gate Pulse Width Necessary To Trigger</td>
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<tr>
<td>Gate Trigger Current</td>
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<tr>
<td>Gate Trigger Voltage</td>
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<tr>
<td>Peak On-State Voltage</td>
</tr>
</tbody>
</table>
| Conventional Circuit Committed Turn-Off Time$^{(1)}$ (With Reverse Voltage) | | - | 45 | 50 | μsec | (1) $T_c = + 125^\circ C$
(2) $I_t = 1000$ amps
(3) $V_r \geq 50$ volts
(4) Rate of Rise of Forward Blocking Voltage $= 200$V/μsec to 80% $V_{D_{RM}}$ or $400$V/μsec to 70% of $V_{D_{RM}}$
(5) Gate Bias = Open During Turn-Off Interval 0 Volts, 100 ohms.
(6) Duty Cycle $\leq 0.01\%$
| Conventional Circuit Committed Turn-Off Time$^{(1)}$ (With Feedback Diode) | | - | 50 | 55 | μsec | (1) $T_c = +125^\circ C$
(2) $I_t = 1000$ amps
(3) $V_r = 2$ Volts Min.
(4) Rate of Rise of Forward Blocking Voltage $= 400$V/μsec to 80% $V_{D_{RM}}$
(5) Gate Bias = Open During Turn-Off Interval
(6) Duty Cycle $\leq 0.01\%$

(1) Turn-off times are measured on a go/no-go basis using LEM test equipment. Experimental determination of critical turn-off times may lead to device degradation.

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1. **MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH AT $T_C = 65^\circ C$ FOR SINUSOIDAL CURRENT WAVEFORMS**

2. **MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH AT $T_C = 90^\circ C$ FOR SINUSOIDAL CURRENT WAVEFORMS**
3. ENERGY PER PULSE FOR SINUSOIDAL PULSES

4. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR $T_C = 65^\circ C$

5. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR $T_C = 90^\circ C$

NOTES:
1. Switching capability and losses with bypass diode.
2. Switching voltage from 15 Volts to 0.8 $V_{DRM}$.
3. Snubber discharge < 50 Amps. RC time constant < 10 $\mu$sec.
4. High gate drive, 20V/10 Ohms, 0.5 $\mu$sec rise time.

6. ENERGY PER PULSE FOR TRAPEZOIDAL CURRENT WAVEFORMS

NOTES:
1. Switching voltage from 15 Volts to 0.8 $V_{DRM}$.
2. DI/DT during turn-on: 100A/$\mu$sec.
3. Reverse voltage < 50 Volts. If no bypass diode is used, recovery switching losses must be added.
4. RC snubber time constant < 10 $\mu$sec.
5. High gate drive: 20V/10 Ohms, 0.5 $\mu$sec rise time.

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7. FORWARD CONDUCTION CHARACTERISTIC
ON-STATE

8. RECOVERED CHARGE (125°C)

NOTES:
If no bypass diode is used with this thyristor, the switching losses during
recovery can be significant. The actual magnitude of these losses will
vary widely depending on circuit conditions and snubber design.
The switching losses in a given circuit may be calculated with
the following equation: \[ SLR = \int_0^\infty t \cdot V(t) \cdot I(t) \, dt \]
Where SLR is the recovery switching losses; \( I(t) \) is the recovery current
decay; \( V(t) \) is the recovery voltage; and \( t = 0 \) occurs at the peak of
the recovery current. \( I(t) \) may be expressed as an exponential decay:
\[ I(t) = I_{pe} \cdot e^{-(t/T)} \]
Where \( I_{pe} \) is the peak recovery current and
\( T = 2.5\mu s \). The junction temperature rise
due to the recovery losses may be computed
as follows:
\[ \Delta T_j = F \cdot \sigma_{ja} \cdot R_{thJA} \cdot \alpha \cdot A \cdot 3.5 \]
Where \( \sigma_{ja} \) is the recovery losses,
\( R_{thJA} \) is the DC junction to ambient thermal impedance,
and \( F \) is the operating frequency.

This curve represents the maximum recovery loss as a function
of circuit \( dI/dt \), and different assumed linear \( dv/dt \)s.

9. RECOVERY CURRENT
SWITCHING LOSSES

10. TRANSIENT THERMAL RESISTANCE –
JUNCTION-TO-CASE

NOTES:
1. Add .006°C/W to account for both case to dissipator
interfaces when properly mounted; e.g., \( R_{thJC} = 0.029 \)
C/W. See Mounting Instructions.
2. DC Thermal Impedance is based on average full cycle
junction temperature.
**11. GATE TRIGGER CHARACTERISTICS AND POWER RATINGS**

When the Press-Pak is assembled to a heat sink in accordance with the following general instructions, a reliable and low thermal resistance interface will result.

1. Check each mating surface for nicks, scratches, flatness and surface finish. The heat dissipator mating surfaces should be flat within .0005 inches and have a surface finish of 63 micro-inches.

2. It is recommended that the heat dissipator be plated with nickel or tin. Bare aluminum or copper surfaces will oxidize in time resulting in excessively high thermal resistance.

3. Sand each surface lightly with 600 grit paper just prior to assembly. Clean off and apply silicone oil (GE SF1154 200 centistoke viscosity) or silicone grease (GE G623 or Dow Corning DC3, 4, 340 or 640). Clean off and apply again as a thin film. (A thick film will adversely affect the electrical and thermal resistances.)

4. Assemble with the specified mounting force applied through a self-leveling, swivel connection. The force has to be evenly distributed over the full area. Center holes on both top and bottom of the Press-Pak are for locating purposes only.