Type C792 thyristor is suitable for phase control applications such as for HVDC valves, static VAR compensators and synchronous motor drives. The silicon junction design utilizes a second generation pilot gate and a unique orientation of emitter shorts which promote the lateral expansion of conducting plasma resulting in lower spreading losses while achieving high dv/dt withstand. It is supplied in an industry accepted disc-type package, ready to mount using commercially available heat dissipators and mechanical clamping hardware.

MECHANICAL OUTLINE

ELECTRICAL
CREEPAGE / STRIKE
1.6 / 1.0 in
40.6 / 25.4 mm
CLAMPING FORCE
(range)
17000–19000 lb.
<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MAXIMUM VALUES</th>
<th>UNIT S</th>
</tr>
</thead>
<tbody>
<tr>
<td>Repetitive peak off-state and reverse voltage</td>
<td>V_{DRM} V_{RRM}</td>
<td>T_j=0 to +115°C</td>
<td>see table</td>
<td>V</td>
</tr>
<tr>
<td>Repetitive working crest voltage</td>
<td>V_{DWM} V_{DRM}</td>
<td>T_j=0 to 115°C</td>
<td>.8 V_{RRM} V_{DRM}</td>
<td>V</td>
</tr>
<tr>
<td>Rep.off-state and reverse leakage current</td>
<td>I_{DWM} I_{RRM}</td>
<td>V_{DWM} V_{RRM}</td>
<td>150 ma 150 ma</td>
<td>ma</td>
</tr>
<tr>
<td>On-state Voltage</td>
<td>V_{TM} I_{2000A} T_j=115°C</td>
<td>I_{2000A} T_{p}=8.3ms T_{j}=115°C</td>
<td>1.90 V</td>
<td>V</td>
</tr>
<tr>
<td>Critical DC gate current/voltage to trigger on</td>
<td>I_{GT} V_{GT}</td>
<td>V_{25°C}</td>
<td>150 ma 3</td>
<td>ma V</td>
</tr>
<tr>
<td>Non-trigger gate current/voltage</td>
<td>I_{GD} V_{GD}</td>
<td>V_{25°C}</td>
<td>0.67 V_{RRM} V_{DRM}</td>
<td>8 ma</td>
</tr>
<tr>
<td>Critical rate of rise of off-state</td>
<td>dv/dt</td>
<td>T_{j}=115°C</td>
<td>0.67 V_{RRM} T_{j}=115°C</td>
<td>2000 V/us</td>
</tr>
<tr>
<td>Critical rate of rise of on-state</td>
<td>di/dt</td>
<td>T_{j}=115°C</td>
<td>0.67 V_{RRM} T_{j}=115°C</td>
<td>100 A/us</td>
</tr>
<tr>
<td>Peak recovery current</td>
<td>I_{recovery}</td>
<td>0.67 V_{RRM} T_{j}=115°C</td>
<td>118 A</td>
<td></td>
</tr>
<tr>
<td>Peak half-cycle non-repetitive surge current</td>
<td>I_{TSU}</td>
<td>T_{p}=8.3ms T_{p}=10 ms</td>
<td>35 kA 34</td>
<td></td>
</tr>
<tr>
<td>Circuit commutated turn-off time</td>
<td>t_{q}</td>
<td>0.5 di/dt=5A/us T_{p}=10-20 ms</td>
<td>600 us</td>
<td></td>
</tr>
</tbody>
</table>

GATE CIRCUIT REQUIREMENTS

Open circuit voltage: 40 - 50 V
Short circuit current: 3 A minimum
Current risetime: 0.5 us nominal
Pulse duration: 10-20 us
**Gate Characteristics and Gate Supply Requirements**

- **THYRISTOR GATE IMPEDANCE**
  Enhanced by fast rising gate voltage, increasing anode bias and junction temperature. It is at a minimum for dc current, zero anode bias and low temperature.

- **GATE SUPPLY**
  Prefer 50V/10 ohm for supporting the di/dt rating and life expectancy. The short circuit current risetime should be nominally 0.5us and the duration longer than the expected delay time for all magnitudes of anode bias. Practically 10-30us is recommended followed by a back porch of 750ma if needed to sustain conduction.

- **MINIMUM ACCEPTABLE GATE CURRENT**
  The intersection of the load line and gate impedance characteristic indicates the minimum value of actual current needed during the delay time interval to support di/dt. A different load line meeting this criterion may be used.

- **MAXIMUM GATE RATINGS**
  Peak gate power, $P_{gm(100us)} = 300$ W
  Average gate power, $P_{g(av)} = 50$ W
  Peak gate current, $I_{gfm} = 25$ A
  Peak reverse voltage, $V_{grm} = 25$ V

---

**Non-Repetitive Surge Current and I2t for Fusing**

- $I_{t_{sm}}$ (kA)
- $I_2t$ Mamp2sec
- $I_{t_{sm}}$ and $I_2t$ are determined by the intersection of the graph and the relevant characteristics.