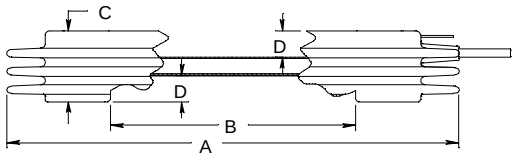
SILICON POWER

SPT227
1650A, 4500V
77mm Thyristor

Features
1650A, 4500V
26kA Surge Rating Capability
Light Weight Package

Package
A=4.437in, B=2.50in, C=0.797in, D=0.306in
Notes - 1, 2 & 3



Description
Type SPT227 reverse blocking thyristor is suitable for phase control applications A unique pilot gate and orientation of emitter shorts are employed which promote lower plasma spreading losses and high dv/dt withstand. It is manufactured by the proven multi-diffusion process.
The design utilizes the revolutionary "Light Silicon Sandwich" or LSS technology, a new termination technique which eliminates heavy refractory metal as a substrate but still employs the alloyed anode interface necessary for high surge current duty. The light weight plastic package allows the insertion of liquid cooled chillers closer to the silicon junction. Copper inserts can be supplied for adjoining commercially available flat surfaced heat dissipators.

MODEL RATING AVAILABILITY

PART NUMBER	V_{DRM}	V_{RRM}
SPT227HK	4500	4500
SPT227HH	4400	4400
SPT227HF	4300	4300
SPT227HD	4200	4200
SPT227HB	4100	4100
SPT227FT	4000	4000

Limiting Characteristics and Ratings
At T_J = 125°C, Unless Otherwise Specified

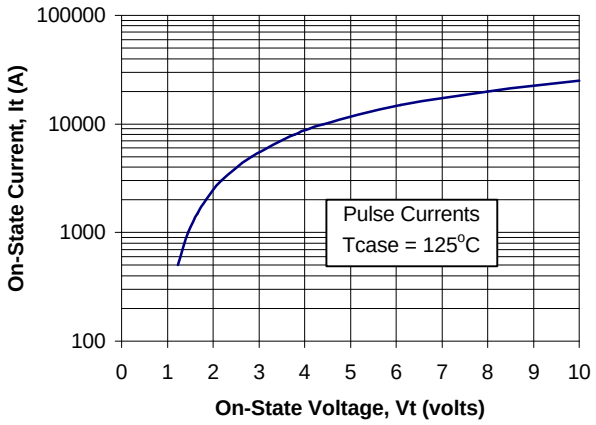
	SYMBOL		UNITS
Repetitive Peak Off State Voltage	V_{DRM}	4500	V
Repetitive Peak Reverse Voltage	V_{RRM}	4500	V
Average On-State Current (T_C=70°C)	$I_{T(AV)}$	1650	A
Peak Half-Cycle Non-Repetitive Surge Current (8.3ms / 10ms)	I_{TSM}	26 / 24	kA
For Fusing (8.3ms / 10ms)	I^2t	2.8 / 2.9	MA^2s
Critical Gate Trigger Voltage (V_D = 12V, T_J = 25°C)	V_{GT}	4.5	V
Critical Gate Trigger Current (V_D = 12V, T_J = 25°C)	I_{GT}	300	mA
Non-Trigger Gate Voltage (V_D = 2000V)	V_{GD}	0.8	V
Non-Trigger Gate Current (V_D = 2000V)	I_{GD}	15	mA
Open Circuit Gate Voltage	V_{OC}	40	V
Short Circuit Gate Current	I_{SS}	4	A
Gate Pulse Duration and Rise Time	10 µs duration / 0.5 µs rise time		
Turn-Off Time (5A/µs, >100V, 400V/µs to 2000V)	Toff	400	µs
Turn-On Delay (V_D = 50%V_{DRM})	td	3	µs
Rate of Change of Voltage (V_D=70% V_{DRM})	dv/dt	1000	V/µs
Rate of Change of Current (V_D=50% V_{DRM})	di/dt	125	A/µs
Operating and Storage Temperature	T_J, T_{STG}	0 to +125	°C
Mounting Force	F	6000 - 7500	lbs

Notes
1. Optional external posts dwg. # 21528332; Ni plated copper, 0.35" thick each.
2. Compressed thickness including external posts is 0.88" - 0.89" (22.35mm - 22.61mm).
3. Weight XX oz., XX lbs with posts.

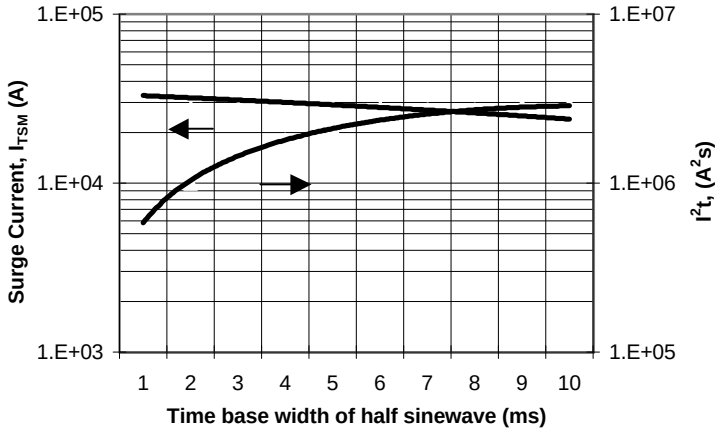
Electrical Specifications
At T_J = 125°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Peak Off State Blocking	I_{DRM}	V_D = 80%V_{DRM}			300	mA
Forward & Reverse Current	I_{RRM}				200	mA
On State Voltage	V_{TM}	I_T = 2000A Pulse			1.85	V
Max. Peak Recovery Current	I_{RM}	di/dt = 2A/µs Snap. S = .5-.33			62	A
Thermal Resistance	$R_{\theta JC}$	Double Side Cooling			0.01	°C/W

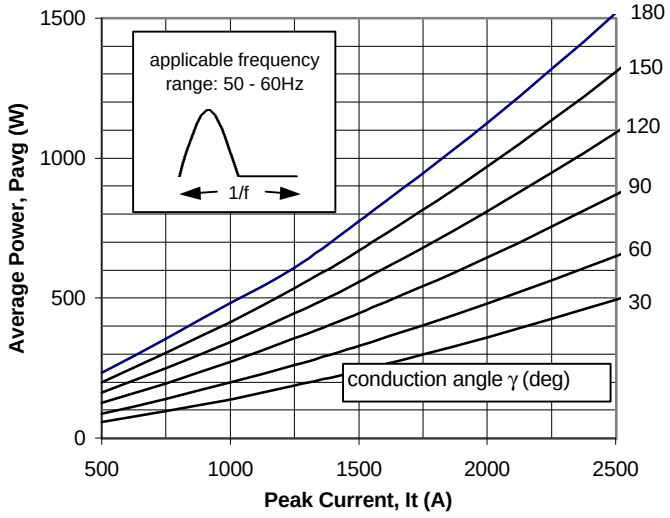
Limiting Performance Curves

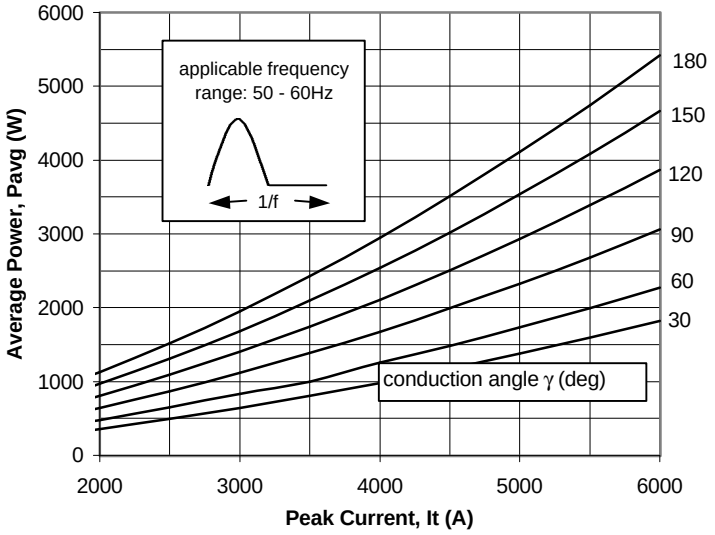


ON-STATE CURRENT CHARACTERITIC



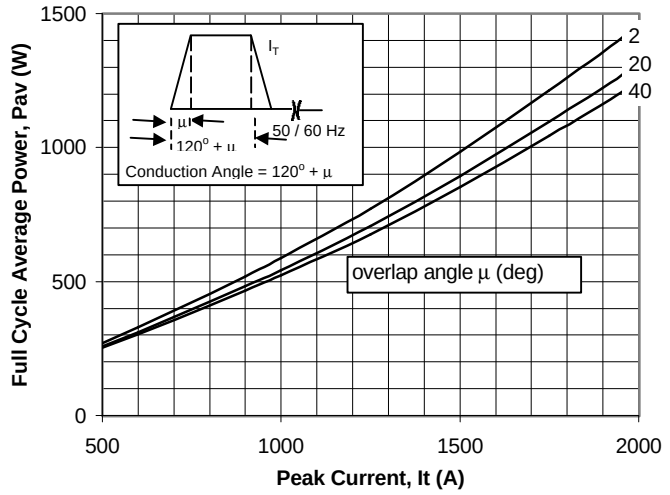
NON-REPETITIVE I_{TSM} AND I^2t CAPABILITY FOR FUSE COORDINATION

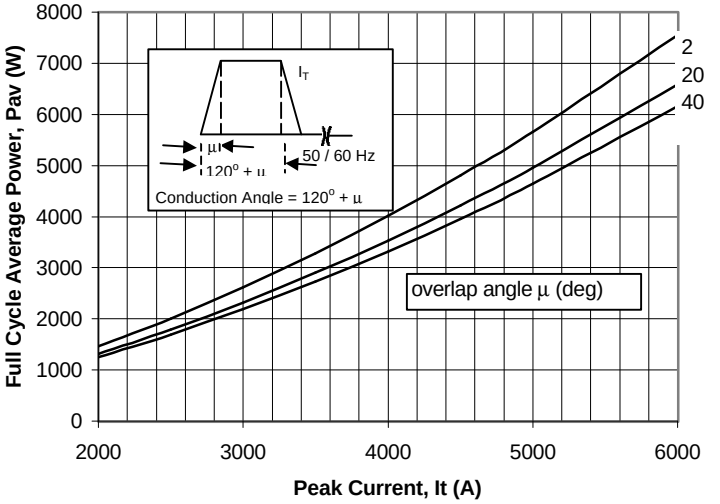




MAXIMUM FULL CYCLE AVERAGE POWER DISSIPATION SINE WAVE CURRENT FOR VARIOUS CONDUCTING ANGLES

PLASMA SPREADING LOSSES ARE INCLUDED.

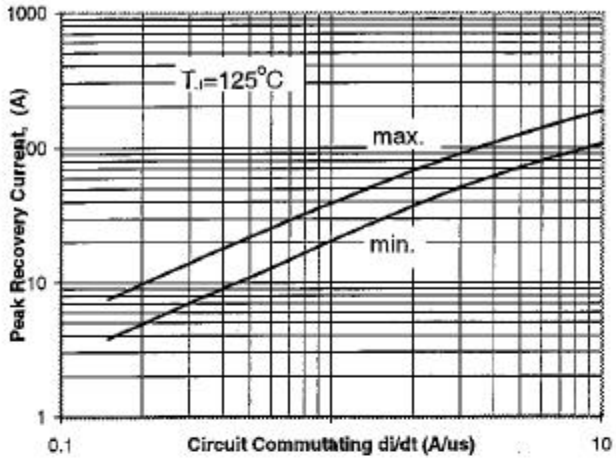


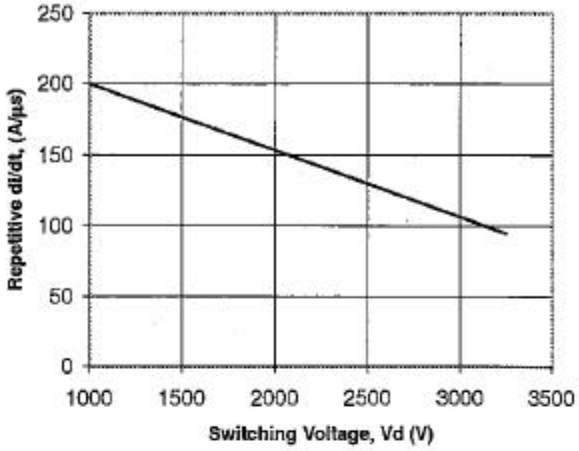


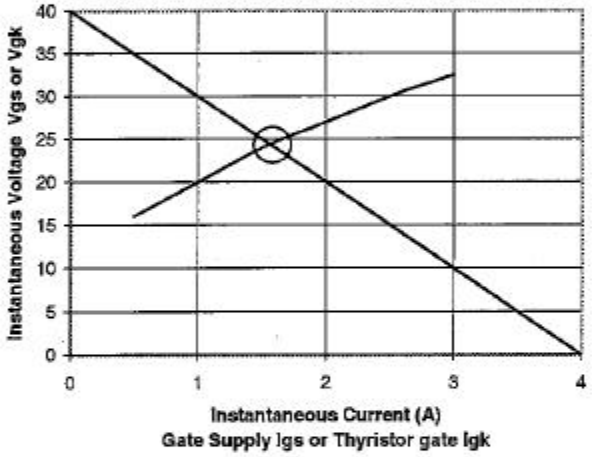
MAXIMUM FULL CYCLE AVERAGE POWER DISSIPATION FOR THREE PHASE RECTIFIER AT SPECIFIED OVERLAP ANGLES, "μ"

. PLASMA SPREADING LOSSES ARE INCLUDED.

Limiting Performance Curves







Thyristor Gate Impedance

- This is enhanced by fast rising gate voltage, increasing anode bias and temperature.
- It is minimum for dc voltage, zero anode bias and low temperature *(not shown)*.

Gate Supply

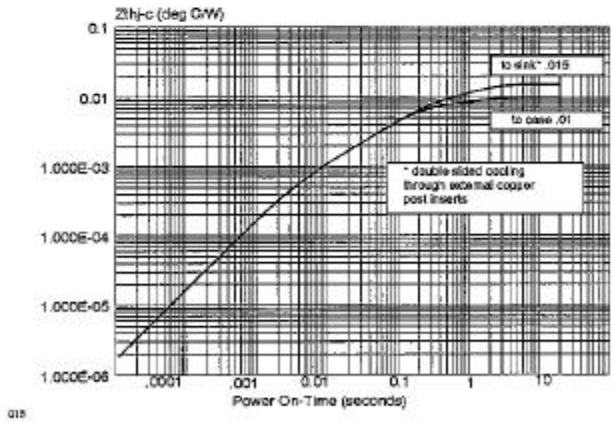
- Load line 40V / 10Ω is recommended when full di/dt_{rep} rating is expected in service. The short circuit risetime should be approximately 0.5µs and and the duration longer than the expected delay time for the thyristor, in most cases 10 -20 µs.

Minimum Acceptable Gate Current

-The intersection of load line and gate characteristic, shown encircled, indicates the minimum value of actual current flowing into the gate of the thyristor needed high di/dt and industrial life.

Maximum Gate Ratings

- peak gate power, P_{GM} (100µs) ----------250 W
- average gate power, $P_{G(av)}$ ----------25 W
- peak gate current ----------20 A
- peak reverse voltage, V_{GRM} ----------20 V



THERMAL IMPEDANCE vs POWER ON TIME

Notes:

1.The LSS package has recessed interfaced cups rather than solid poles allowing for the direct insertion of chiller posts. However, nickel plated copper posts are provided which fill the recesses for joining to flat surfaces,.

2. It is essential that any inserted posts are prepared to the same flatness specifications as the inset posts (dwg. 21526332) provided

3. It is recommended that the external mechanical spring clamps have an adequate displacement (30 - 60 mils) and that steel (STL) force spreaders be at least 1/2" thick and of proper hardness, e.g. 220 - 240 Bhn. This function may be provided by a rigid heat sink.

4. Assembly design should consider avoiding wrenching of bus bars under heavy faults currents, inductively coupled circulating currents and corona effects.