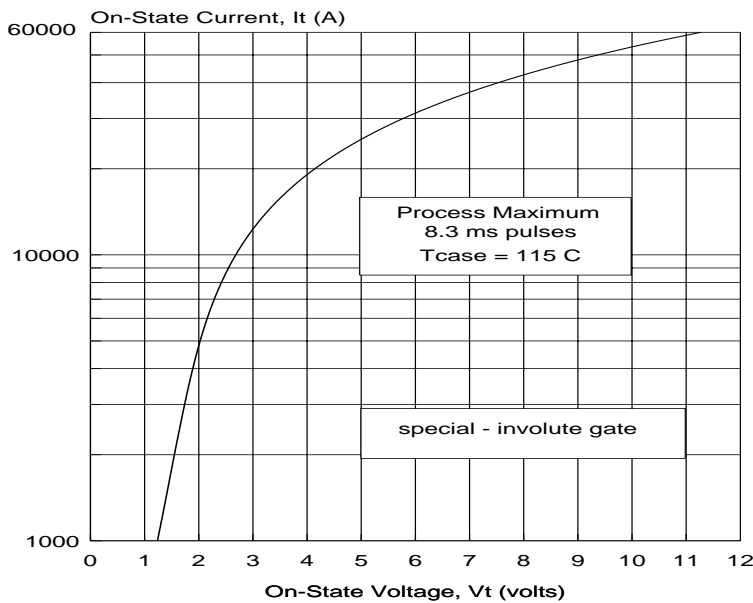


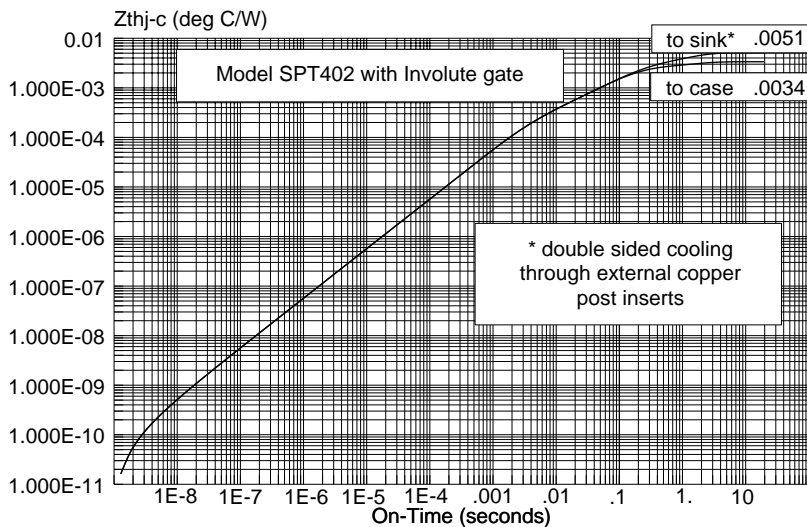
The SPT402 thyristor features a multi-arm involute gate which can be triggered with 5 - 10 A gate pulses by means of an integrated pilot gate or directly fired using 50 - 100A gate pulses. The involute pattern affords full area conduction in minimum time while a corresponding high di/dt rating depends on the choice of gating method. The factory setting for either pilot triggered or gate triggered version, internal to the package, is an option when ordering by keying it to the model number code. The design utilizes a new termination technique, SPCO's revolutionary Light Silicon Sandwich, LSS technology, which eliminates heavy refractory metal as a substrate while retaining the alloyed anode interface necessary for high surge current duty. This thyristor is supplied in a **reliable plastic light weight package** allowing the insertion of liquid cooled chillers. Solid copper inserts can be ordered for adjoining air cooled heat dissipators using commercially available clamping hardware.

ON-STATE CHARACTERISTIC Process Maximum



96h:t402onst

THERMAL IMPEDANCE vs. ON-TIME



96h:12/11/96

96h:pm4

Maximum Off-State & Reverse Blocking Voltage Ratings

$T_J = 0 \text{ to } 115^\circ\text{C}$

V_{DRM} (volts) V_{RRM}

SPT402_HT	5000	5000
SPT402_HS	4900	4900
SPT402_HR	4800	4800
SPT402_HP	4700	4700
SPT402_HM	4600	4600
SPT402_HK	4500	4500

Internal gate connection:

Pilot SPT402A (see page 2 for gate drive)
Direct SPT402B " "

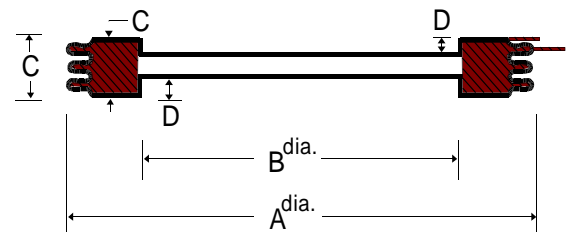
External clamping force
25000 lb minimum

Optional external posts drw. # 0215B8315

Ni plated copper, 0.35" thick each

Compressed thickness including external posts
0.87" - 0.88"

Weight: 18oz without posts
3 lb 10 oz with posts



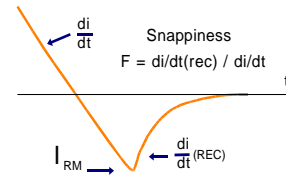
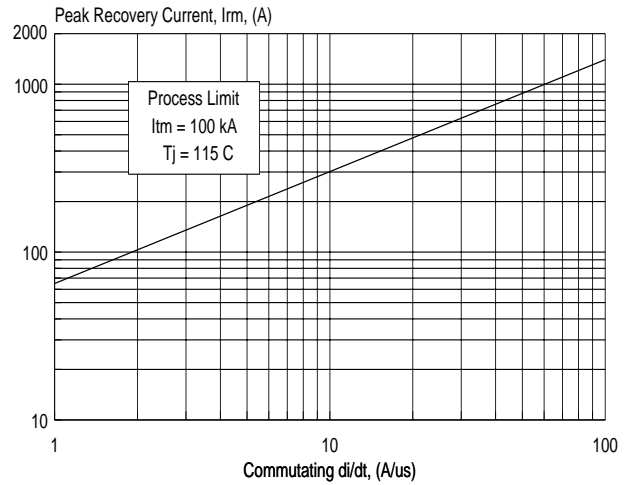
Nominal Dimensions

	inch	mm
A dia.	6 13/32	162.7
B dia.	4 3/16	106.4
C	51/64	20.24
D	0.3061	7.77

LIMITING CHARACTERISTICS AND RATINGS

Repetitive peak off-state & reverse volts	V_{DRM} V_{RRM}	$T_j=0$ to 115°C	up to 5000	V
Repetitive working crest voltage	V_{DWM} V_{RWM}	$T_j=0$ to 115°C	$0.8V_{DRM}$ $0.8V_{RRM}$	V
Repetitive peak off-state & reverse current	I_{DWM} I_{RWM}	$T_j=0$ to 115°C	250 100	ma
Average on-state current	$I_{T(AV)}$	$T_{amb} = 70^\circ\text{C}$	4600	A
Peak half-cycle non-rep surge current	I_{TSM}	8.3 ms 1.5 ms $T_j=115^\circ\text{C}$	60 100	kA
On-state voltage	V_{TM}	$I_c=4000\text{A}$ $t_p=8.3\text{ms}$ $T_j=115^\circ\text{C}$	1.90	V
Critical gate trigger current / voltage	I_{GT} V_{GT}	$V_D = 12\text{V}$ $T_j = 25^\circ\text{C}$	150 5.0	ma V
Non-trigger gate current	I_{GD} V_{GD}	$V_D = 2000\text{V}$ $T_j = 115^\circ\text{C}$	15 0.8	ma V
Maximum peak recovery current	I_{RM}	$di/dt = 2\text{A/us}$ $T_j = 115^\circ\text{C}$	110 snappiness	A $F = 2-3$
Critical rate of rise of on-state current	di/dt_{rep}	$T_j=115^\circ\text{C}$ 60 Hz incl. 60A snubber discharge	SPT402A 100 SPT402B 400	A/us
Critical rate of rise of off-state voltage	dv/dt	$T_j=115^\circ\text{C}$ $V_D = 67\% V_{DRM}$	1000	V/us
Turn-on delay	t_a	$V_D = 50\%V_{DRM}$ $T_j=115^\circ\text{C}$	4	us
Turn-off time	T_{off}	5A/us, -100V 20V/us to 2000V	400	us

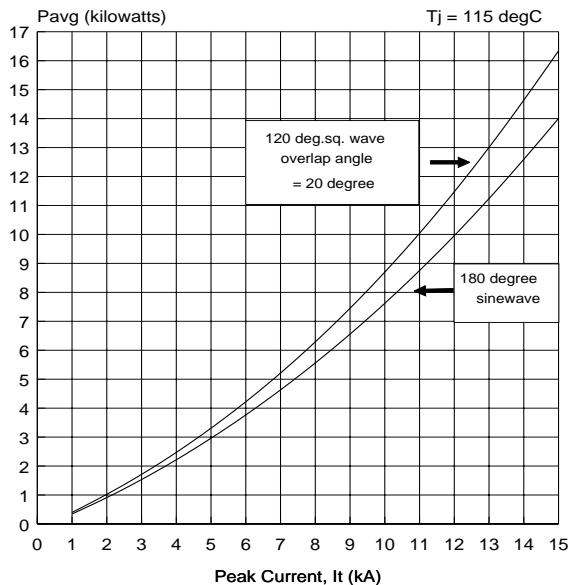
Peak Recovery Current Relationship with Commutating di/dt



Gate Pulse: 15us duration / 0.5us rise time
SPT402A SPT402B

				di/dt	$\leq 100\text{A/us}$	$< 1000\text{A/us}$	$1000-4000\text{A/us}$
				V_{OC}	50 V	100 V	100 V
				I_{SS}	5 A	200 A	400 A

FULL CYCLE AVERAGE POWER LOSS versus PEAK CURRENT at 50/60 Hz (plasma spreading and conduction loss)



FULL CYCLE AVERAGE POWER LOSS 50 / 60 Hz $T_j = 115^\circ\text{C}$

I_T (peak) amperes	half-sine 180° watts	3ph 120° watts
1000	369	424
2000	921	1035
3000	1547	1727
4000	2233	2493
5000	2978	3331
6000	3783	4246
7000	4650	5241
8000	5580	6319
9000	6577	7483
10000	7641	8735
11000	8775	10078
12000	9981	11516
13000	11259	13048
14000	12612	14679
15000	14042	16408