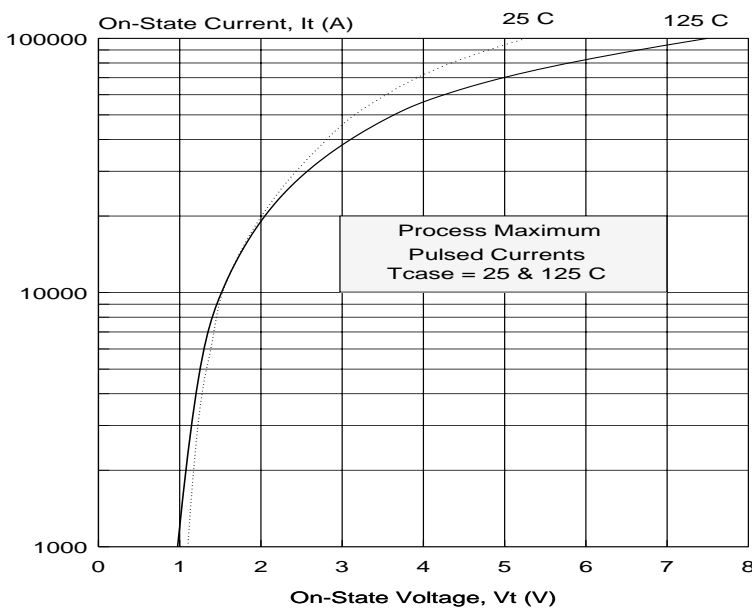


Type SPT407 thyristor is optimized especially for pulse power and static transfer switch applications for which lowest on-state voltage is achieved. The silicon junction utilizes a second generation pilot gate and a unique orientation of emitter shorts which promote the lateral expansion of conducting plasma resulting in lower spreading losses while achieving high dv/dt withstand. It is supplied in a **reliable plastic light weight package** using SPCO's revolutionary "Light Silicon Sandwich", **LSS** technology, a new termination technique which eliminates heavy refractory metal as a substrate while retaining an alloyed anode interface necessary for high surge current duty. External posts are available for adjoining commercially available heat dissipators using clamping hardware.

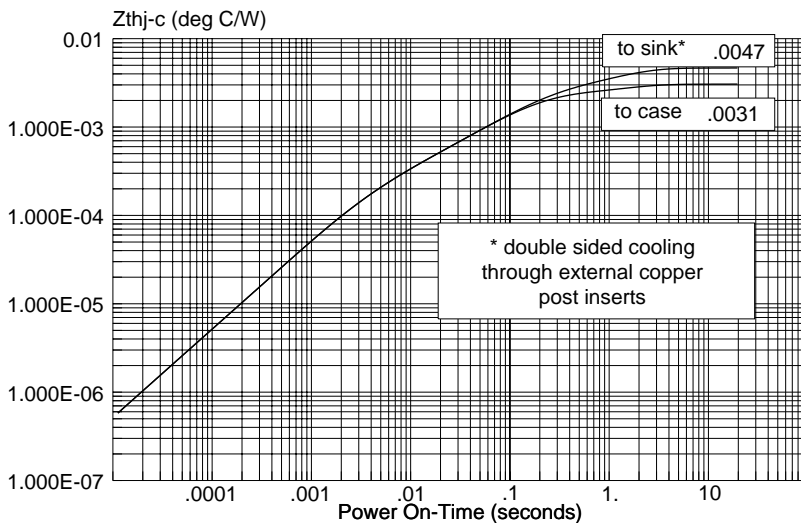
ON-STATE CHARACTERISTIC

Process Maximum



97f:

THERMAL IMPEDANCE vs. ON-TIME



7/1/97 rev 96d:

97f:pm5

Maximum Off-State & Reverse Blocking Voltage Ratings

$T_j = 0 \text{ to } 115^\circ\text{C}$

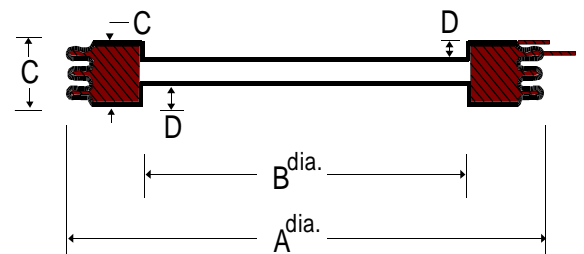
| | V_{DRM} (volts) | V_{RRM} |
|----------|-------------------|-----------|
| SPT407DK | 2500 | 2500 |
| SPT407DH | 2400 | 2400 |
| SPT407DF | 2300 | 2300 |
| SPT407DD | 2200 | 2200 |
| SPT407DB | 2100 | 2100 |
| SPT407TT | 2000 | 2000 |

External clamping force
25000 - 30000 lb

Optional external posts drw.# 0215B8315
Ni plated copper, 0.35" thick each.

Compressed thickness including external posts
0.86" - 0.87"

Weight: 18 oz
3 lb 10 oz with posts



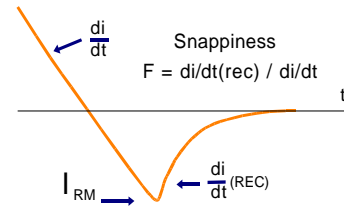
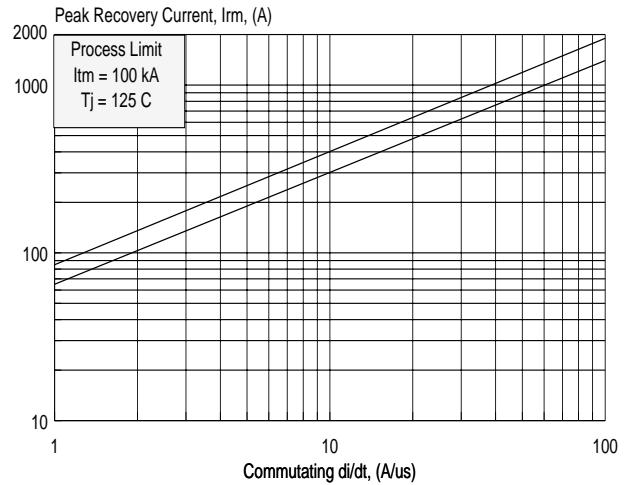
Nominal Dimensions

| | inch | mm |
|--------|---------|-------|
| A dia. | 6 13/32 | 162.7 |
| B dia. | 4 3/16 | 106.4 |
| C | 51/64 | 20.24 |
| D | 0.3149 | 8.00 |

LIMITING CHARACTERISTICS AND RATINGS

| | | | | |
|---|------------------------|--|-----------------------------|---------|
| Repetitive peak off-state & reverse volts | V_{DRM} V_{RRM} | $T_j=0$ to 115°C | up to 2500 | V |
| Repetitive peak off-state & reverse current | I_{DRM} I_{RRM} | $T_j=0$ to 115°C | 450 60 | ma |
| Average on-state current | $I_{T(AV)}$ | $T_{case} = 70^\circ\text{C}$ | 7525 | A |
| Peak half-cycle non-rep surge current | I_{TSM} | 8.3 ms 1.5 ms $T_j=115^\circ\text{C}$ | 100 150 | kA |
| On-state voltage | V_{TM} | $I_T=4000\text{A}$ $T_j=115^\circ\text{C}$ | 1.20 | V |
| Critical gate trigger current / voltage | I_{GT} V_{GT} | $V_D = 12\text{V}$ $T_j = 25^\circ\text{C}$ | 150 3.0 | ma V |
| Non-trigger gate current | I_{GD} | $V_D = 2000\text{V}$ $T_j = 115^\circ\text{C}$ | 15 | ma |
| Maximum peak recovery current | I_{RM} | $di/dt = 2\text{A/us}$ $T_j = 115^\circ\text{C}$ | 130 snappiness $F = 2-3$ | A |
| Critical rate of rise of on-state current | di/dt_{rep} | $T_j=115^\circ\text{C}$ 60 Hz with 60A snubber discharge | 100 | A/us |
| Critical rate of rise of off-state voltage | dv/dt | $T_j=115^\circ\text{C}$ $V_D = 67\% V_{DRM}$ | 1000 | V/us |
| Turn-on delay | t_a | $V_D = 50\%V_{DRM}$ $T_j=115^\circ\text{C}$ | 4 | us |
| Turn-off time | T_{off} | 5A/us, -100V 20V/us to 2000V | 300 | us |

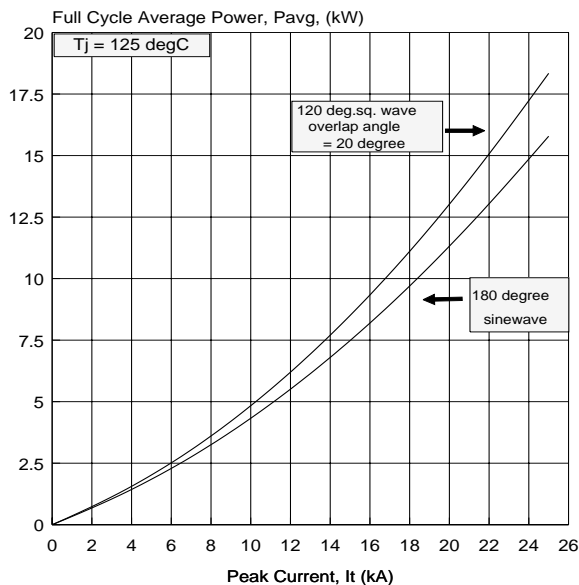
Peak Recovery Current Relationship with Commutating di/dt



Recommended gate drive to sustain turn-on di/dt rating

$V_{OC} = 50\text{V}$
 $I_{SS} = 5\text{A}$
 rise time = 0.5 us
 duration 10 - 20 us

FULL CYCLE AVERAGE POWER LOSS versus PEAK CURRENT at 50/60 Hz (plasma spreading and conduction loss)



FULL CYCLE AVERAGE POWER LOSS 50 / 60 Hz $T_j = 125^\circ\text{C}$

| I_T (peak) amperes | half-sine 180° watts | 3ph 120° watts |
|----------------------|----------------------|----------------|
| 2500 | 823 | 885 |
| 5000 | 1814 | 1979 |
| 7500 | 2972 | 3284 |
| 10000 | 4298 | 4800 |
| 12500 | 5792 | 6527 |
| 15000 | 7454 | 8466 |
| 17500 | 9285 | 10617 |
| 20000 | 11284 | 12979 |
| 22500 | 13451 | 15554 |
| 25000 | 15787 | 18341 |