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Voltage Controlled Solidtron – Trigger Circuits

1.0 VCS Gate trigger considerations

Driving Voltage Controlled Solidtrons (VCS) is similar to driving power MOSFETs or IGBT devices, but with a few important differences. VCS devices require a negative gate bias to guarantee Off-State; additionally they are also latching devices. Another important difference is that VCS devices cannot hard turn-off high levels of switch conduction current (anode-cathode current). For example, the SMCTTA32N14A10 devices can turn-on up to 4kA for a short time (~ 1uS), but can only force commutate (turn-off) 30A of switch conduction current. Once a VCS is triggered and the device will almost immediately latch until either the current self-commutates and a negative gate bias is applied or force commutated with a negative gate bias at low conduction current levels. Solidtrons are best suited for fast pulse discharge applications where large energy is discharged in a short time and the conduction current is allowed to ring down to zero.

1.1 Negative gate bias

Min. negative bias recommended for all models of VCS to guarantee Off-State: -5V
Absolute Max. Gate bias voltage for all models of VCS: +/- 25V

1.2 Gate capacitance

Triggering a VCS device essentially involves slewing the voltage across the input capacitance (gate-cathode) from a negative bias voltage to a positive voltage. The input capacitance varies with VCS device model and can be found listed under performance characteristics in the datasheet for that particular device type. Generally, most applications for Solidtrons do not apply high anode-cathode dv/dt while the VCS device is in the off state, but in cases where there is high dv/dt to the anode-cathode voltage, one must also consider the gate-anode (miller) capacitance, which tends to significantly increase the total gate charge requirement.

1.3 Parasitic Inductance

Apart from the parasitic capacitance careful attention must be given to minimize the parasitic gate inductance. Significant inductance in the gate circuit could result in high gate voltage transients, which could puncture the oxide layer on the VCS device gate thus destroying the gate. Use of a 15V Transient Voltage Suppressor (TVS) close to the gate adds a measure of protection. But good layout design practices like, maintaining short distances between traces, shielding, gate-gate return current loop orientation to switch current, wide traces, etc. can virtually eliminate the problem in most applications.

1.4 Separate gate return

The VCS devices are designed for high di/dt applications, thus all VCS device packages (TO-247, ThinPak® and F-pak®) provide an independent cathode connection or Gate Return (GR). It is generally recommended that a separate return path be used for the gate drive to minimize the effects of rapidly changing anode-cathode current on the gate control voltage.

2.0 Gate Trigger Circuits

Although there are several similarities in driving a MOSFET or IGBT when compared to VCS devices, it is important to note that the high levels of voltage and currents involved in typical solidtron applications, present some unique challenges. Many topologies could be utilized to trigger VCS devices for a variety of applications; however, two particular designs with key benefits are highlighted in this document. The first design features low off-state power dissipation and the second design features simplicity. A third design for driving series connected VCS devices is not covered in

this document. Driving Current Controlled Solidtron (CCS) devices are also covered in a separate document (S5002).

2.1 Design 1 - Totem Pole Topology

The first circuit shown in Figure 1 is a fully isolated gate trigger circuit with an optional boost stage. The recommended Agilent optical isolator (HCNW3120-300) is also a fully integrated gate drive rated at 2A peak current, which is suitable for many VCS applications. However, if faster turn-on is needed, it is necessary to include a boost stage (S1 and S2 in Figure 1) in the gate drive design. The boost stage provides high peak gate current for faster turn-on of the VCS device. When the trigger signal is low S2 is closed and S1 is open to provide a negative bias to the VCS gate. When the trigger signal is high S1 closes and S2 opens connecting the VCS gate to the positive rail.

Power is provided by an isolated DC power supply (Vaux can be 10 or 12V supply). Diode D2 clamps the positive rail voltage to +5V and the remaining voltage (~7V if using a 12V supply) is seen at the negative rail. This method restricts power supply voltage transients to the negative rail. The topology minimizes power consumption when the solidtron device is in the off state.

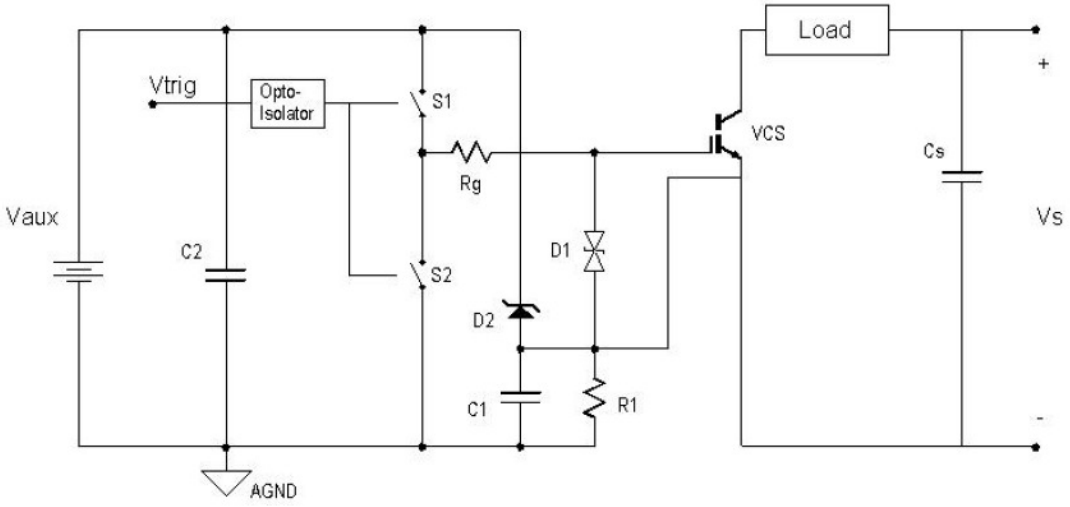

Figure 1. Fully isolated gate trigger circuit.

D2 : 5V zener
D1 : +/-15V TVS protects the MOS gate from excessive gate voltage transients.
S1, S2 (optional) : S1 is open and S2 is closed when Vtrig is low and S1 is closed and S2 is open when Vtrig is High (e.g. Fairchild FDS4559 Complimentary HEXFET devices)
Vaux: Isolated 12V DC power supply. (e.g. Burr-Brown DCV00512)
Vtrig : Usually from 0 to 5V TTL compatible signal. An Agilent Technologies HCNW3120-300 or a similar optical isolator provides isolation for the trigger circuit.
Rg : Limits current to S1 or S2 Ipk.
C1: 0.1uF, 60V
C2: 2.2uF, 25V

2.2 Design 2 – Single Switch Topology

The single switch design only uses a single MOSFET switch (see S1 in Figure 2) to trigger the Solidtron device. A series of resistors maintains a small positive voltage at the anode while maintaining the gate

potential at zero. The R1, R2 and R3 resistor network is such that R1=R, R2=2R and R3=0.5R. Selecting the value of R is application specific. The value of R controls the rate at which the capacitor Cg charges and also the off state power dissipation. Thus the selection of the value R is a trade off between how quickly Cg charges (t = (R1+R3).Cg)and how much power can the application be allowed to waste in the off state (higher values of R reduces off –state power dissipation). The resistor network divides the voltage from the isolated DC supply (Vaux) such that the anode of the Solidtron is maintained at 1/7th Vaux while the voltage across the capacitor Cg is 4/7th Vaux. When Vtrig goes high, S1 closes connecting the gate of the VCS device to the capacitor Cg. This discharges the charge stored in Cg (Q=Cg.4/7th Vaux) to the VCS gate and triggers the VCS into the on state. Once anode current is established in the Solidtron, the device latches until the anode current rings down to zero and device self commutates by re-establishing a positive voltage at the anode.

One of the key advantages of this topology is due to the fact that the gate remains grounded when the VCS device is in the off state. Additionally, fewer components are used in the drive circuit and the use of a single isolated dc supply is an important benefit. The primary drawback of this circuit is the higher off-state power requirement.

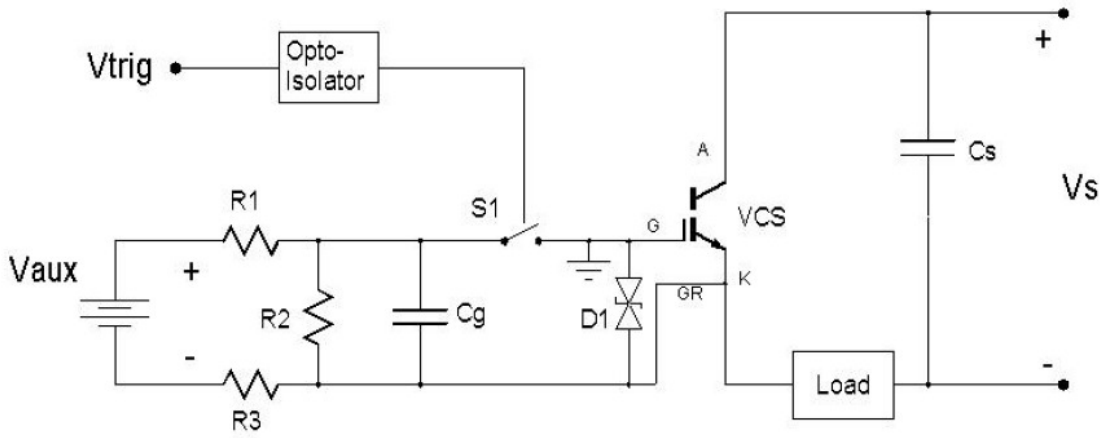

Figure 2 Single switch VCS trigger circuit.

R1: R (see text)
R2: 2 x R
R3: 0.5 x R
Cg: 0.2 uF, 100V
D1: +/-15V TVS protect the VCS MOS gate from excessive gate voltage transients.
Q1: Any 100V, 8A peak drain current MOSFET (e.g. International Rectifier IRLL110)
Vaux: Isolated DC power supply can range between 18 to 25 VDC
Vtrig : Usually from 0 to 5V TTL compatible signal. Optical isolator provides isolation for the trigger circuit (e.g. Agilent 4N25 series).