

NOTICE: This product is export controlled

The **SP205-01** is an ultra-fast high-voltage thyristor packaged in an **F-Pak** custom SMT package. The **SP205-01T** is identical to the SP205-01 with the exception that its pads have been robotically tinned with 63Sn-37Pb solder prior to final testing.

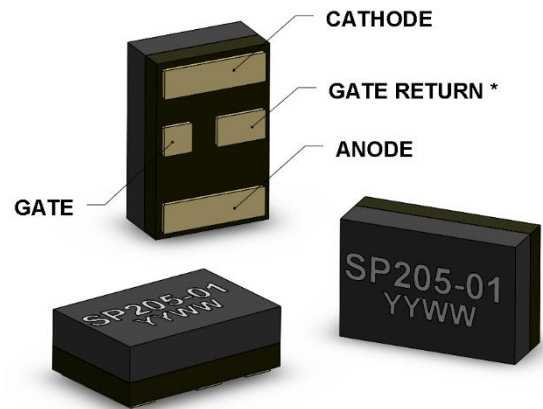
As with all Solidtron products, the core semiconductor employs high cell density and an advanced termination design to achieve high peak current capability, low turn-on & conduction loss, very low off-state leakage, negligible turn-on delay jitter, and extremely high turn-on dI/dt capability.

The **F-Pak** is an application-specific surface mount package in which the semiconductor is “flip-chip” soldered onto a multilayer high temperature PCB substrate. The **F-Pak** uses no wire bonds. Instead, the anode is connected to the PCB substrate using a soldered copper lug. The assembly is then epoxy underfilled and encapsulated using Hysol FP4651 epoxy.

The **F-Pak** offers a very small footprint and low inductance interface that allows for high volume installation using conventional SMT handling equipment. This product is specifically intended for use as an initiator firing switch and is a superior alternative to triggered spark gaps.

Key Product Features

- 1500V Repetitive Off-State Voltage
- Off-State Leakage Current $\leq 1.0\mu\text{A}$ @ 1500V @ 85°C
- $V_{GK} = 0\text{V} = \text{OFF-STATE}$
- 120 kA/ μs dI/dt capability
- Low Turn-on and Conduction Losses
- < 60nSec Turn-on Delay Time
- 3kA Repetitive Surge Current



*The **Gate Return** pad provides a dedicated connection directly to the cathode of the semiconductor die.

Using the Gate Return pad as an independent gate driver return path reduces $V=L*dI/dt$ induced stress on the gate driver components.

The Gate Return pad of this product may, alternatively, be used as an additional Cathode connection; however, using it in this fashion must be qualified by the customer for their specific application.

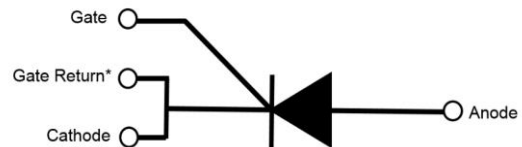


Table 1. Maximum Ratings

	Symbol	Value	Units
Repetitive Peak Off-State Anode Voltage	V_{DRM}	1500	V
Repetitive Peak Reverse Anode Voltage	V_{RRM}	-10	V
Off-State Rate of Change of Voltage Immunity ($V_D=1500\text{V}$)	dv/dt	1000	V/ μSec
Non-Repetitive Surge Current (1/2 Sinusoid, Pulse Duration $\leq 200\text{nSec}$)	I_{TSM}	3500	A
Repetitive Surge Current (1/2 Sinusoid, Pulse Duration $\leq 200\text{nSec}$)	I_{TRM}	3000	A
Rate of Change of Current	dI/dt	120	kA/ μSec
Critical Capacitor Discharge Event Integral (Underdamped LCR Circuit) (Note 1.)	$I^2t_{CRITICAL}$	1.18	A ² sec
Repetitive Capacitor Discharge Event Integral (Underdamped LCR Circuit) (Note 1.)	$I^2t_{REPETITIVE}$	1.0	A ² sec
Repetitive Peak Reverse Gate Blocking Voltage	V_{RGM}	-5	V
Forward Gate Current ($\leq 10\mu\text{Sec}$ Duration, Square Waveform)	I_{GM}	10	A
Operating Junction Temperature Range	T_J	-55 to +125	°C
Maximum Guaranteed Off-State Gate Voltage		0	V
Maximum Soldering Installation Temperature (See Moisture Sensitivity Caution)		220	°C
Storage Temperature Range (See Moisture Sensitivity & Solderability Cautions)		-55 to +150	°C

Note 1. Unique characteristic associated with initiator firing – see application notes

Table 2. Electrical Characteristics

Parameter	Symbol	Test Conditions	Measurements				
			Min	Typ	Max	Units	
Anode to Cathode Breakdown Voltage	V_{BR}	$V_{GK} = 0V, I_D = 100\mu A, T_C \leq 125^\circ C$	1500			V	
Anode-Cathode Forward Off-State Current <i>See Figure 1.</i>	I_{DRM}	$V_{GK} = 0V, V_D = 1500V$	$T_C = -55^\circ C$		80	nA	
			$T_C = 25^\circ C$		12	100	nA
			$T_C = 85^\circ C$		120	1000	nA
			$T_C = 125^\circ C$		3.5	15	μA
Reverse Bias Gate-Cathode Breakdown Voltage	V_{GRRM}	$I_{GM} = 500\mu A, T_C \leq 125^\circ C$	5			V	
Four Volt Reverse Bias Gate-Cathode Leakage Current	I_{GM}	$V_{GK} = -4V$	$T_C = 25^\circ C$		250	μA	
			$T_C = 85^\circ C$		300	μA	
			$T_C = 125^\circ C$		350	μA	
Two Volt Reverse Bias Gate-Cathode Leakage Current	I_{GM}	$V_{GK} = -2V$	$T_C = 25^\circ C$		60	μA	
			$T_C = 85^\circ C$		75	μA	
			$T_C = 125^\circ C$		100	μA	
Gate Trigger Voltage	V_{GT}	$V_D = 12V, I_D = 1mA$	$T_C = 25^\circ C$	450	500	mV	
			$T_C = 85^\circ C$	250	350	mV	
			$T_C = 125^\circ C$	200	250	mV	
Gate Trigger Current	I_{GT}	$V_D = 12V, I_D = 1mA, T_C \leq 125^\circ C$			100	μA	
Turn-on Delay Time	$t_{d(ON)}$	0.10 μF Capacitor Discharge,		30	60	nSec	
Rate of Change of Current	dI/dt	$T_C = 25^\circ C, I_{GT} = 500mA,$		65		kA/ μsec	
Capacitor Discharge Event Integral	I^2t	$V_{DD} = 1200V, L_S = 15nH,$		0.92		A ² sec	
Peak Anode Current	I_{DM}	$R_S = 0.010\Omega = CVR$		2.7		kA	

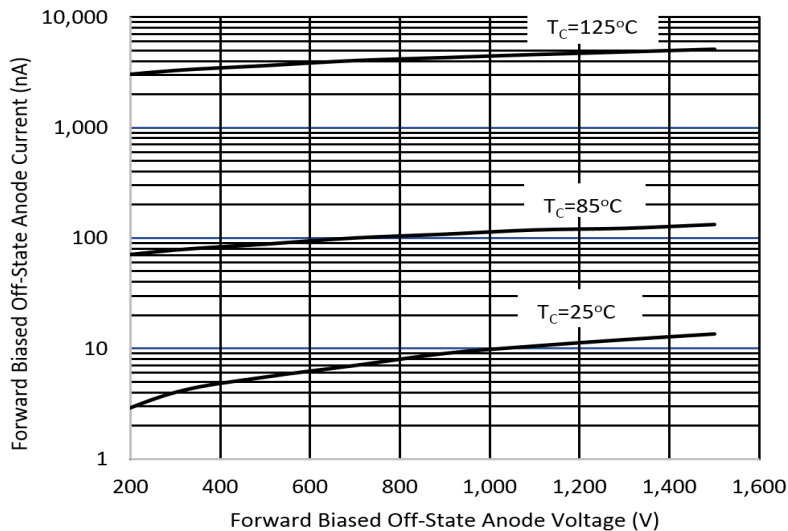


Figure 1. Typical Forward Biased Off-State Anode-Cathode Leakage Characteristic

ESD Sensitivity

The **SP205-01/SP205-01T** have been tested IAW **MIL-STD-883 ESD-HBM (Human Body Model)** to **+/-2000V (Class 1C)**.

The **SP205-01/SP205-01T** have been tested IAW **ANSI/ESDA/JEDEC/JS-002-2014 for ESD-CDM (Charged Device Model)** to **+/-1500V (Class C5)**.

Moisture Sensitivity

The **SP205-01/SP205-01T** have been tested IAW **IPC/JEDEC J-STD-020** and are classified as **MSL Level 4**.

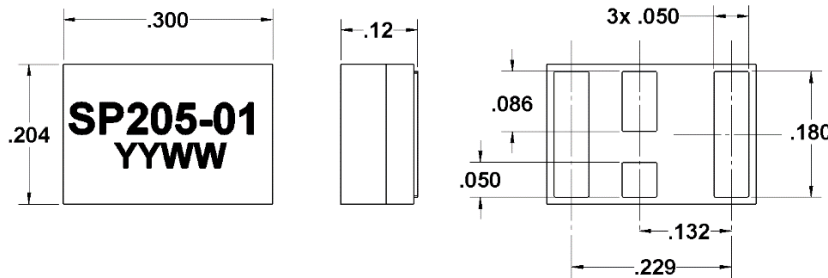
In accordance with **IPC/JEDEC J-STD-033, F-Pak** products are dry-baked and immediately packed in a Moisture Barrier Bag (MBB) containing desiccant and a Humidity Indicator Card (HIC). When the Moisture Barrier Bag is opened or compromised refer to **IPC/JEDEC J-STD-033** for proper HIC interpretation, floor life and storage procedures.

Although **IPC/JEDEC J-STD-033** prescribes specific dry-baking temperatures and times, caution is advised as additional baking of **F-Pak** SMD packages may cause oxidation and/or intermetallic growth of the terminations which may result in solderability problems during board installation. The temperature and time for baking this SMD package should, therefore, be limited with solderability considerations in mind. If available, it is recommended F-Paks be baked in a nitrogen or vacuum oven to limit exposure to oxygen during the baking process.

Solderability

SP205-01 - Although the component pads appear to be gold plated, exposure to high process temperatures within the manufacturing process have accelerated the diffusion of the underlying nickel into and through the thin exterior gold surface, therefore, rendering the pads **subject to oxidation growth** if exposed to circumstances which promote nickel oxidation. Such circumstances should be avoided; otherwise, solderability of the **SP205-01** will be compromised.

SP205-01T – Prior to final electrical testing, the component pads of the **SP205-01T** are **robotically tinned with 63Sn–37Pb solder**. Thickness and coverage is in accordance with **MIL-PRF-38535**. Please note that PbSn solder is also subject to oxidation growth; however, at a slower rate than the underlying nickel. Conventional handling and storage practices associated with components having 63Sn-37Pb tinned leads may be applied.

Markings and Dimensions

DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE

NOTED:

TWO PLACE DECIMAL +/- 0.010"

THREE PLACE DECIMAL +/- 0.005"

PART NUMBER

SP = SILICON POWER

205 = CHIP TYPE

-01 = PACKAGE TYPE

DATE CODE

YY = LAST 2 DIGITS OF CALENDAR YEAR

WW = WORK WEEK

NOTE: The "T" in Part Number SP205-01T **WILL NOT** be ink marked on the plastic package of the component itself. The presence of solder on its pads, rather than gold plating, is the only differentiating characteristic between the SP205-01 and the SP205-01T. Shipping trays, Moisture Barrier Bags and other packing labels WILL include the "T" as the final digit of the Part Number.

Ordering Information

The **SP205-01** and **SP205-01T** are priced differently and are subject to different lead times. Be certain to specify the complete part number and description listed in Table 3. when requesting a quotation or placing an order.

Table 3. Ordering Information

Part Number	Description	Qty per Tray
SP205-01	Solid State Initiator Firing Switch, F-Pak, Ni/Au pad finish	88
SP205-01T	Solid State Initiator Firing Switch, F-Pak, 63Sn-37Pb pad finish	88

Application Notes

Available

- [Triggering a Current Controlled Solidtron \(CCS\) Device](#)

Under Development

- Gate Driver designs for the CCS Device
 - Suggested Circuits & Critical Layout Considerations
- Capacitor Discharge Event Integral (i^2t)

Table 4. Typical Application Parameters

	Value	Units
Off-State Anode Voltage (<1 hour)	1250	V
Repetitive Peak Forward Anode Current (1/2 Cycle Pulse Width = 160nSec)	2.7	kA
Repetitive Peak Reverse Anode Current (1/2 Cycle Pulse Width = 160nSec)	2.2	kA
Off-State Rate of Change of Voltage (dv/dt) immunity	≤2.2	V/mSec
Operational Case Temperature	-55 to 85	°C
Rate of Change of Anode Current (di/dt)	65	kA/μSec
Peak Forward Gate Current (≤20uSec pulse)	500	mA
Event Repetition Rate	<1	Hz

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This product is not designed, intended or authorized for use in applications intended to save or sustain life, specifically those in which the failure of this product could create a situation where personal injury or loss of life may result. Should a customer purchase or use this product for any such unintended and unauthorized application, the customer shall indemnify and hold **Silicon Power Corporation** and its officers, employees, subsidiaries, affiliates and distributors harmless regarding all claims, costs, damages and expenses associated with any claim of personal injury or death associated with unauthorized use even if such a claim alleges **Silicon Power Corporation** was negligent regarding the design or manufacture of this product.

End users of this product shall comply with all applicable DOD, ITAR, EAR, USML laws and regulations.