PCN20191114 Testing and Analysis Overview

Introduction: The following report documents a process change incorporated into the SP205-01 wafer production process with the objectives of improving product consistency and yield. This report also describes the testing and analysis performed to quantify the potential impact of the process change. This work was completed with the assistance and technical oversight of the Defense Microelectronics Activity (DMEA).

Background: The post processing steps utilized in the manufacture of the SP205-01 include a cleaning procedure designed to remove residual fabrication process material from the wafer back-side prior to final back-metal deposition. The current process demonstrates inconsistent results that vary from wafer-to-wafer, in the removal of processing constituents such as silicon dioxide, silicon nitride, and photoresist residues. The current cleaning process is comprised of the following steps:

- Dry Plasma Etch (Performed by Microchip): Designed to remove residual impurities from the p-type substrate.
- In-Situ Plasma Etch (Performed by LGA): Designed to remove native oxide prior to backside metal deposition.

Etch recipes used in the current process are not optimized for photoresist removal, thus, a varying amount of photoresist residue remains on each wafer after this process is complete. Additionally, material re-deposition during plasma etching results in thin film residue being present on the wafer back-side upon culmination of the current process. The residue left on the wafer back-side is generally identifiable by optical microscopy analysis. However, some of the residual material is only detectable by prohibitively complex advanced beam microscopy analysis methods. Thus, under normal production circumstances, its effects are not realized until after final metal deposition. This results in a detrimental impact on finished wafer yield, in some cases whole wafers are disqualified.

Due to the original process proving to be insufficient at consistently removing all process residue, an additional back grinding step has been introduced into the SP205 wafer production flow which completely removes all processing residues, and subsequently improves overall product quality.

Back grinding is the lowest risk solution capable of removing all process residues, as it does not negatively impact the fabrication layers of the device and avoids the introduction of potential reliability issues such as chemical contamination or oxidation inherent in other mitigation strategies. In addition, the following quality benefits are derived from implementation of the back-grinding step into the process flow:

- The ground silicon surface improves backside emitter contact, backside metal adhesion to the substrate, and ensures optimal solder quality due to the absolute removal of all oxide, nitride and organic residues prior to back-backside metal deposition.
- A uniform substrate thickness (700µm) is achieved, resulting in more consistent electrical and mechanical performance of the substrate material. Previous unground wafers varied between 710µm and 755 µm.

Updated Process: The following changes have been implemented to the wafer back-side processing steps prior to metal deposition:

- No change: Dry Plasma Etch (Microchip). Redundant due to implementation of back grinding step; however, left in process due to the expense of changing the process at Microchip.
- Added: Wafer back-grind to 700µm overall thickness (GDSI)

- No change: In-situ plasma etch (LGA) – Performed under high vacuum in same chamber as final metal deposition.

Validation of Updated Process: In cooperation with the Defense Microelectronics Activity (DMEA), Silicon Power designed and implemented the following methodology to ensure that no adverse electrical, reliability, or mechanical impact was introduced to SP205 production wafers.

- Optical/ Scanning Electron Microscopy (5 samples): Used to detect evidence of potential fracture or lattice dislocation resultant from the back-grinding process
- Energy Dispersive X-Ray Spectroscopy Analysis (5 samples): Used to verify the presence of potentially detrimental elemental constituents on the back side of the sample die.
- Electromagnetic Signature Analysis (5 samples-Packaged): Used to determine if the back-grinding process negatively impacted the substrate stress profile to a degree that electrical performance would be degraded.
- Temperature cycling (30 Samples): Used to propagate any undetected micro-cracking potentially induced by the back-grinding process. The devices were cycled 100 times between -55C and +125C prior to exposure to discharge testing.
- Electrical performance testing before and after temperature cycling (30 Samples): Performed standard SP205-01 battery of tests which includes capacitor discharge testing at a 1.1 A^2S action cycle rating. Capacitor discharge testing was specifically used to further verify that no major fracture or dislocations in the substrate materialized as a result of temperature cycling. All samples were subjected to 100 discharge events before and after temperature cycling. Back ground devices were subjected to an additional 4,400 discharge events with no failures encountered.
- 1600V @ 25C Forward Off-state Leakage Characterization before and after temperature cycling, (30 Samples): Used to verify that any potential defect resulting from back grinding did not worsen during temperature cycling; thus, degrading the high voltage leakage characteristics of the SP205-01.

Optical Microscopy/SEM Analysis Results: DMEA performed an optical scan of the back side of five representative samples supplied by Silicon Power. DMEA's Leica inspection equipment was utilized at a magnification of up to 100X to inspect the back side of the samples with the objective of detecting indications of gross fracture of the material. *This was not observed on any of the supplied samples*.

Figure 1: Typical Back-Side Optical Image

Figure 1. illustrates the typical results of the optical inspection of the samples. Striation due to back-grinding and surface scratching was observed on all samples.

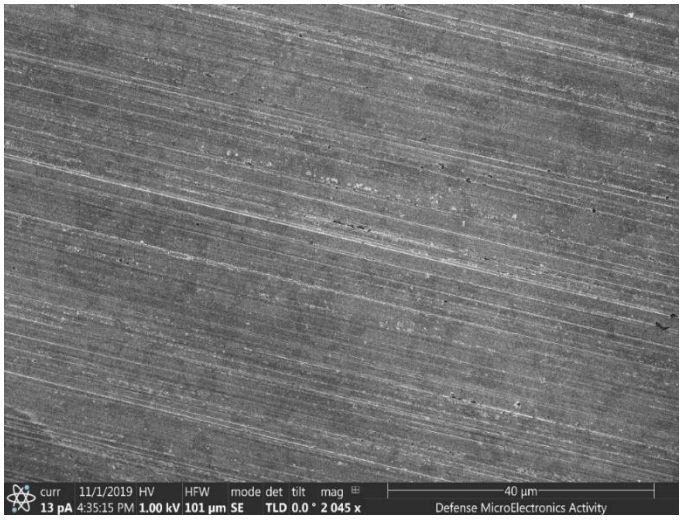

Figure 2: SEM Image of Substrate with Metal

The backside metallization on two samples was removed with an H_2SO_4 etch formulated to leave the Silicon intact (Figure 2).

Following the etch, these samples were inspected utilizing DMEA's FEI dual beam Focused Ion beam (FIB) tool. The objective of this inspection was to detect any signs of micro-cracking originating from the striations left on the samples after back grinding. *No signs of brittle fracture or lattice damage were observed on these samples.*

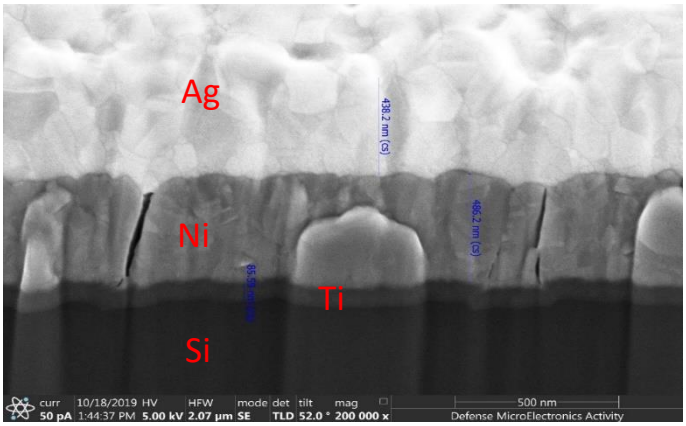

Figure 3: Cross-Section

Following the completion of SEM inspection, an HF-based decoration etch was performed on the two samples with the objective of revealing and highlighting subsurface fracture sites or lattice dislocation. *The samples were then inspected in the SEM (Figure 3.). No signs of brittle fracture were observed*

Focused Ion beam cross sections were taken at random locations on the back side of two remaining samples. Figure 3 illustrates the TI/Ni/Ag plating film thickness.

Figure 4 illustrates a much wider cross section of the substrate area. This was done with the dual purpose of exposing brittle fracture radiating below the surface from striation valleys resultant from the back-grinding process, and to ensure that the sputtered Ti/Ni/Ag plating was within specification. *The plating was found to be within specification, and no radial fracture sites were observed.*

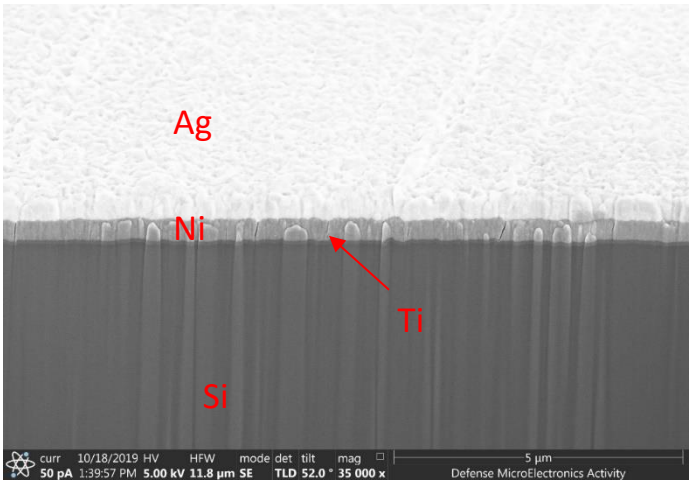

Figure 4: Wide-View Cross-Section (DMEA)

Electromagnetic Signature Analysis Background and Results: All active electronic devices radiate electromagnetic energy that is a characteristic of function and design. Integrated circuits can be characterized by these emission signatures, and changes to these emission signatures. These electromagnetic signatures can be leveraged for many uses. In particular; electromagnetic signature data can be utilized to predict degradation in a circuit due the causal relationship between circuit condition and emission.

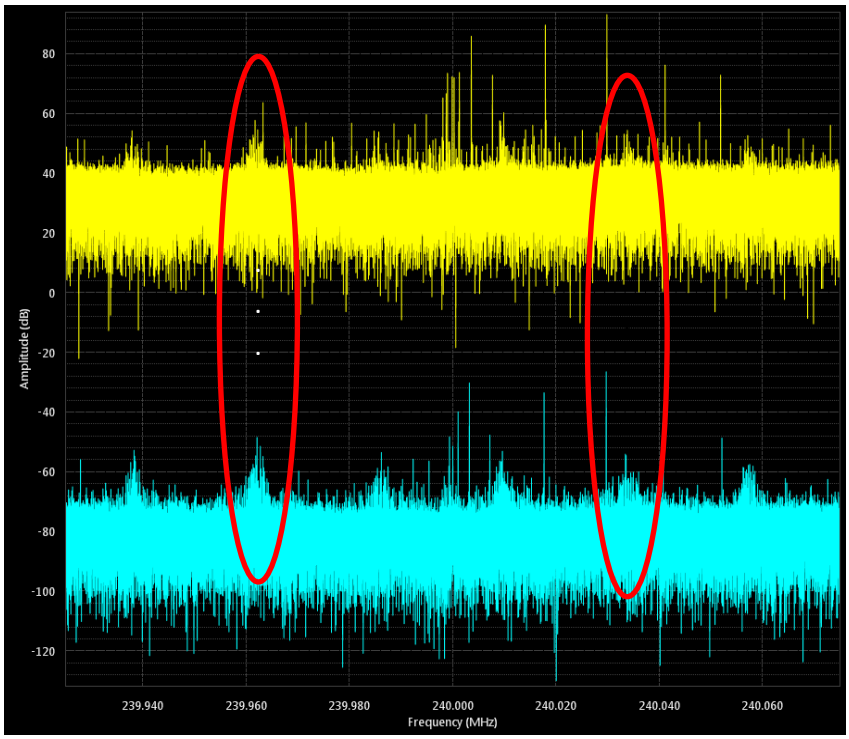

Figure 2: Typical EM Analysis Result: Comparative analysis of the 240 MHz Bandwidth. Known Good Sample (Yellow) and modified (Back Grind) Sample (Blue)

Data acquisition is accomplished using a special sensor with a sensitivity *S*=-170dBm, very close to the theoretical minimum of -173 dBm. Acquisition sweeps typically involve a bandwidth ranging from 30MHz to 3GHz, with 0.01hz to 200Hz Resolution Band Width (RBW). Thus, approximately 10^9 data points are collected from the device-under-test in a typical sweep. Each sweep takes roughly one hour to complete. Changes to multiple signature metrics occur as a device degrades; non-linear mixing product, frequency spacing, element density, peak frequency position, energy distribution, and phase noise attachment all change as a circuit degrades or ages. These changes allow for a quantitative methodology to be adopted to characterize reliability or denote unique failure mechanisms associated with the signature metrics.

DMEA performed EM signature analysis on five representative SP205-01 samples provided by Silicon Power. The results of the broadband sweep of SP205 devices that had undergone back grinding were compared to known good samples that had not undergone back grinding in order to determine the magnitude of any noted degradative effects.

Figure 5 illustrates a typical result for the EM analysis of the samples provided to DMEA by Silicon Power. The blue spectral data represents the emission spectra of a device exposed to back grinding. The yellow spectrum is a device from an earlier date code device that was not subject to back grinding.

Degradative effects typically manifest as large frequency shifts in the fundamental and harmonic content of a degraded component spectral data. Figure 5 clearly shows that the fundamental and harmonic peaks of both signals illustrated in Figure 5 are nearly coincident in frequency. There is a slight increase in the energy density associated with the nonlinear mixing product of the modified sample, indicating that change has occurred in the current flow though the device, when compared to the same sub-bands of the unmodified device (in the sub bands encompassed by the red highlight shown on Figure 5.) However, the absence of major frequency shifts in the fundamental and

harmonic content between the spectral plots illustrated in Figure 5 indicate that *the change due to stress induced by the back-grinding process was minimal.*

Energy Dispersive X-ray Spectroscopy (EDS) Results: DMEA performed EDS analysis at random locations of the back side of three metallized samples provided by Silicon Power with the objective of validating that the back-grinding process had in fact removed residual nitride films used as a mask during wafer fabrication. *The spectral data did not reveal the presence of a nitride film or any contaminant on the analyzed samples.*

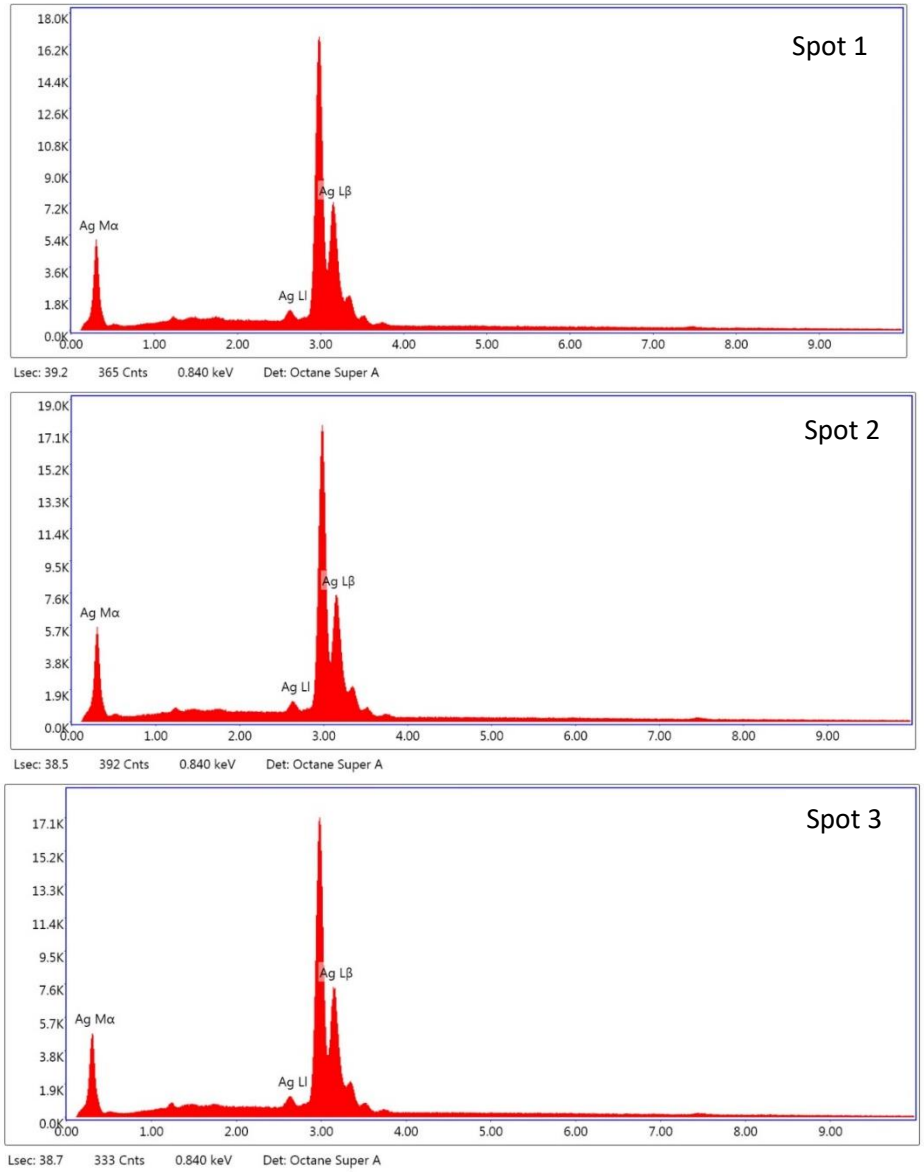

Figure 6: EDS Results Illustrating No Nitrogen Peaks (DMEA)

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Pre-Temperature Cycling SP205-01 Electrical Performance Testing: 30 SP205-01 samples were tested IAW and satisfied the following battery of production tests and a dry-baking cycle.

Description	Conditions	Acceptable Limits
Reverse Bias Gate Integrity Test	T_C = 25˚C, V_{GK} = -5.5V (rectified AC)	$I_{GK(R)}$ ≤ 500µA @ -5V, $I_{GK(R)}$ ≤ 50µA @-2V
125°C 1600V Off-State Leakage Current	T_C = 125˚C, V_{GK} = 0V, V_D = 1600 V	I_{AK} ≤ 4µA
110°C 1600V Off-State Leakage Current, Blocking Stability Verification (3 Minutes)	T_C = 110˚C, V_{GK} = 0V, V_D = 1600 V	I_{AK} ≤ 4µA
Capacitor Discharge (100 Events @ 5pps)	T_C = 25˚C, V_{CC}=1300V, C=0.1µF, L=15nH, I_G=1A	I_{PEAK}≥3kA, $T_{DELAY-ON}$≤100nSec, I2 t=1.1A2s
Gate Trigger Voltage	T_C = 25˚C, V_D = 12V, I_T = >100mA	VGK≥0.45 ≤ 0.6V
J-STD-033 Dry Bake	150˚C, 24hrs. IAW J-STD-033 Table 4-2	N/A
25°C 1600V Off-State Leakage Current	T_C = 25˚C, V_{GK} = 0V, V_D = 1600 V	I_{AK} ≤ 15nA
Reverse Bias Gate Integrity Test	T_C = 25˚C, V_{GK} = -5.5V (rectified AC)	$I_{GK(R)}$ ≤500µA @-5V, $I_{GK(R)}$ ≤ 50µA @-2V

1600V @ 25C Forward Off-state Leakage Characterization: Each of the samples tested in the previous section were tested for 1600V 25C Forward Off-state leakage. Results were recorded for comparison following temperature cycling.

Pre-Temperature Cycling Measurements			
	Off-State Leakage Current 1600V @ 25C w/ VGK=0V		
Sample	1944 (Back-ground)	1935 (Control 2)	1848 (Control 1)
1	3.1nA	3.2nA	3.5nA
2	3.5nA	3.5nA	3.6nA
3	3.3nA	3.4nA	4.9nA
4	3.2nA	3.6nA	5.4nA
5	3.3nA	3.4nA	3.3nA
6	3.3nA	3.4nA	3.4nA
7	3.4nA	3.6nA	3.3nA
8	3.3nA	3.5nA	3.5nA
9	3.4nA	3.4nA	3.6nA
10	3.4nA	3.2nA	5.3nA

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Temperature Cycling Details: DMEA was supplied with 30 previously tested and characterized SP205-01 samples by Silicon Power. These samples were exposed to thermal cycles with the objective of exacerbating and propagating any micro cracking undetectable by inspection. The following parameters were utilized:

- Number of cycles: 100
- Temperature Min: -55C
- Temperature Max: +125C
- Dwell Time at Temperature min/max: 10 min
- Ramp Rate: 5 deg.C/s

To avoid the possibility of destroying all samples if cycled 100 times, two samples from each sub-set were removed after 10, 25 & 50 cycles. The remaining 12 samples were left run the remaining 50 cycles.

- 6 samples (SNs 1 & 2 from each Date Code) subjected to 10 cycles
- 6 samples (SNs 3 & 4 from each Date Code) subjected to 25 cycles
- 6 samples (SNs 5 & 6 from each Date Code) subjected to 50 cycles
- 12 samples (SNs 7-10 from each Date Code) subjected to 100 cycles

Full details of the thermal testing are included in a separate report.

Post-Temperature Cycling SP205-01 Electrical Performance Testing Results: Following temperature cycling, the 30 SP205-01 samples were returned to Silicon Power and retested IAW the standard battery of production tests outlined previously. *All 30 samples performed satisfactorily with no observed change in performance.*

Post-Temperature Cycling 1600V @ 25C Forward Off-state Leakage Characterization Results: Following Performance Testing, each of the 30 samples were again tested for 1600V 25C Forward Off-State leakage. *No discernable changes in leakage performance were seen suggesting that the temperature cycling had not induced additional damage.*

Post-Temperature Cycling Measurements			
	Off-State Leakage Current 1600V @ 25C w/ VGK=0V		
Sample	1944 (Back-ground)	1935 (Control 2)	1848 (Control 1)
1	3.0nA	3.2nA	3.3nA
2	3.5nA	3.4nA	3.4nA
3	3.3nA	3.3nA	4.5nA
4	3.2nA	3.3nA	5.0nA
5	3.2nA	3.3nA	3.4nA
6	3.3nA	3.5nA	3.4nA
7	3.3nA	3.5nA	3.3nA
8	3.3nA	3.5nA	3.4nA
9	3.4nA	3.5nA	3.6nA
10	3.4nA	3.2nA	5.2nA

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Continued Capacitor Discharge Testing Results: Following post-temperature cycling 1600V Leakage characterization, each of the10 back-ground samples from Date Code 1944 were subjected to 4,400 additional capacitor discharge events. *All samples are still fully operational with no observed difference in performance.*

Conclusions:

- Optical Microscopy Inspections of the sample die delivered to DMEA showed no signs of metallization separation due to substrate fracture
- FIB and SEM imaging performed at random sample locations did not detect voiding or radial fracture originating from striation locations. No sub surface fracture or voiding was detected.
- EDS analysis performed on the backside metallization did not detect any residual thin film or chemical contamination.
- Electromagnetic signature analysis results demonstrate that change to the substrate stress profile induced by the back grinding was minimal. This is the paramount reliability concern on a Silicon substrate exposed to a back-grinding process step. Note that the sensitivity of the RF sensor used in this testing is-171dBm; the theoretical minimum for such a sensor is -173 dBm.
- Subsequent electrical characterization by Silicon Power upon completion of temperature cycling clearly demonstrate that device performance and reliability was not compromised by the addition of the back-grinding step

Silicon Power has determined the state of the existing wafer bank necessitates an additional cleaning step be added to improve production yield. Back-grinding has been determined to be the lowest risk method of completely removing process residue prior to final back-side metallization. DMEA tested various dry (plasma) etch techniques to remove the residue and determined that the risk of component damage due to excessive oxidation to be unacceptably high. Exposure of the production wafers to wet chemicals capable of removing organic material carries the potential of ionic contamination and damage to the device passivation layers. Both of these effects would have a negative impact on wafer production yield and intrinsic device reliability.

DMEA has evaluated back-ground SP205-01 samples utilizing a variety of advanced analysis techniques that offer fidelity far beyond traditional electrical characterization and found only slight/negligible differences between the back-ground and non-back-ground SP205-01s. DMEA's analysis fully supports the electrical characterization and test results obtained by Silicon Power. Based on these findings, DMEA concurs with Silicon Power that the addition of back-grinding process step has a negligible impact on the performance and reliability of production SP205-01. DMEA further concurs that the addition of the back-grind process step will result in a more consistent final product, in terms of electrical performance and mechanical properties.

Respectfully,

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